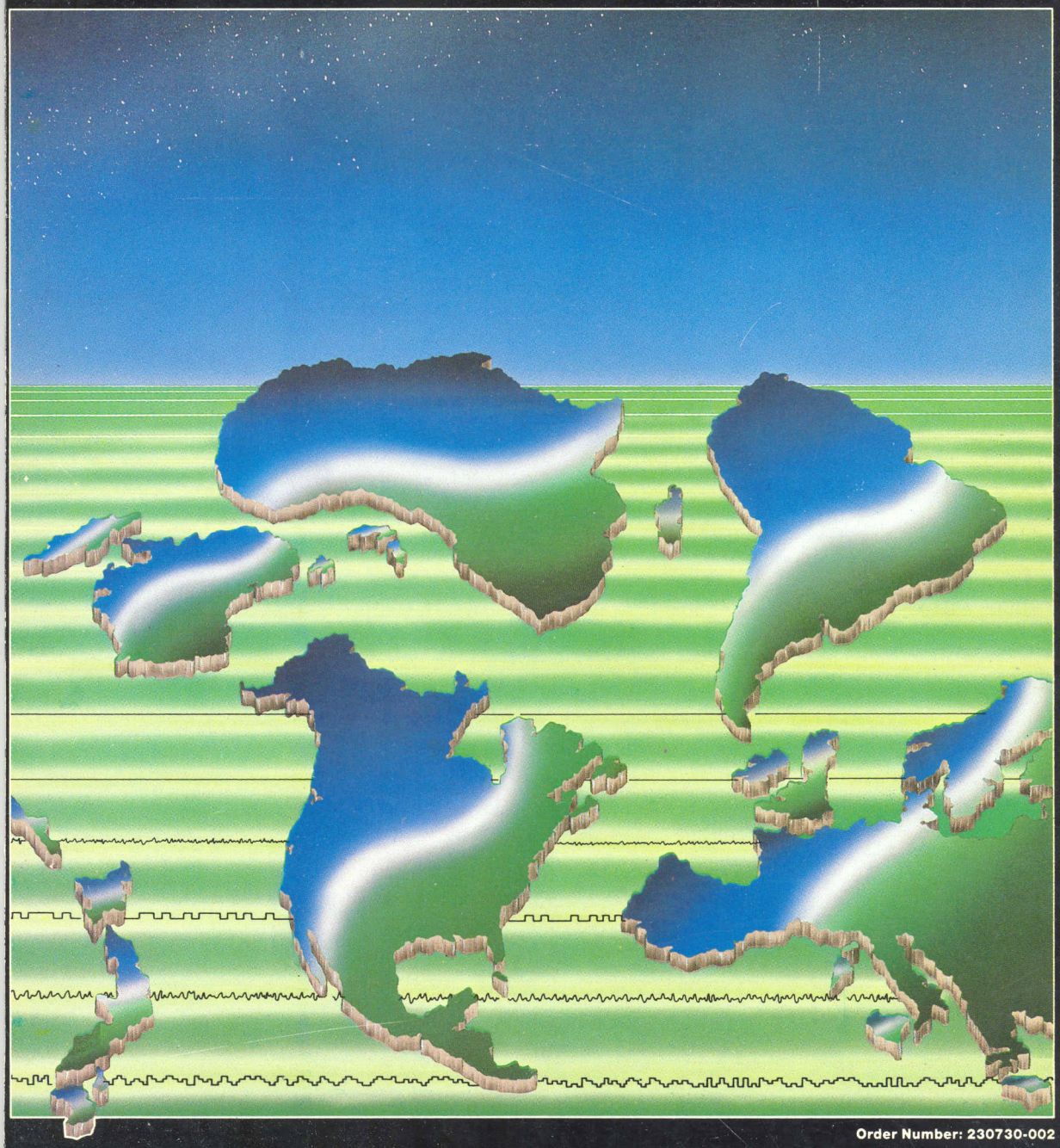
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Telecommunication Products Handbook



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TELECOMMUNICATION PRODUCTS HANDBOOK

1984

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Codecs and Filters 1

1 Codecs and Filters

2910A
PCM CODEC — μLAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G712 Compatible, ATT T1 Compatible with 8th Bit Signaling**
- **Microcomputer Interface with On-Chip Timeslot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots are Used**
- **78 dB Dynamic Range, with Resolution Equivalent to 12-Bit Linear Conversion Around Zero**
- **±5% Power Supplies: +12V, +5V, −5V**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33 mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel 2910A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide in-band signaling.

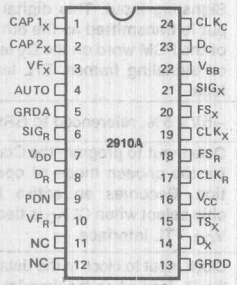
The primary applications are in telephone systems:

- Transmission — T1 Carrier
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

The wide dynamic range of the 2910A (78 dB) and the minimal conversion time (80 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Secure Communications Systems
- Telemetry
- Signal Processing Systems

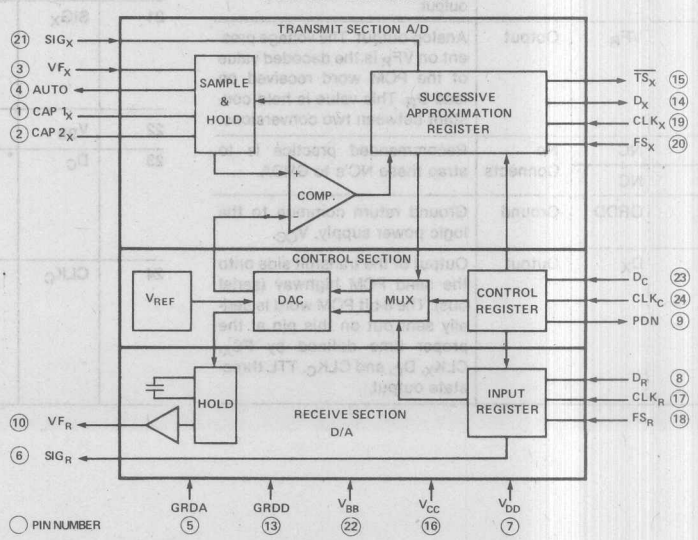
PIN CONFIGURATION



PIN NAMES

$CAP1_X$, $CAP2_X$	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C, SIG_X	Digital Input
SIG_R, D_X, $\overline{TS}_X$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1	$CAP1_X$	Hold	Connections for the transmit holding capacitor. Refer to Applications section.
2	$CAP2_X$		
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for negative, −5V for positive inputs). Refer to the Codec Applications section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
6	SIG_R	Output	Signaling output. SIG_R is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL interface.
7	V_{DD}	Power	+12V ± 5%; referenced to GRDA.
8	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8 bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
9	PDN	Output	Active high when Codec is in the power down state. Open drain output.
10	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions.
11	NC	No Connects	Recommended practice is to strap these NC's to GRDA.
12	NC		
13	GRDD	Ground	Ground return common to the logic power supply, V_{CC}.
14	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
15	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Timeslot information used for diagnostic purposes and also to gate the data on the D_X lead.) Open drain output.
16	V_{CC}	Power	+5V ± 5%, referenced to GRDD.
17	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
18	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Resets the on-chip timeslot counter for the receive side. Maximum repetition rate 12 KHz. Also used to differentiate between non-signaling frames and signaling frames on the receive side. TTL interface.
19	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
20	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Resets the on-chip timeslot counter for the transmit side. Maximum repetition rate 12 KHz. Also used to differentiate between non-signaling frames and signaling frames on the transmit side. TTL interface.
21	SIG_X	Input	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the D_X lead, on signaling frames. TTL interface.
22	V_{BB}	Power	−5V ± 5%, referenced to GRDA.
23	D_C	Input	Data input to program the Codec for the chosen mode of operation. Becomes an active low chip select when CLK_C is tied to V_{CC}. TTL interface.
24	CLK_C	Input	Clock input to clock in the data on the D_C lead when the timeslot assignment feature is used; tied to V_{CC} to disable this feature. TTL interface.

FUNCTIONAL DESCRIPTION

The 2910A PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

In a typical telephone system the Codec is used between the PCM highways and the channel filters.

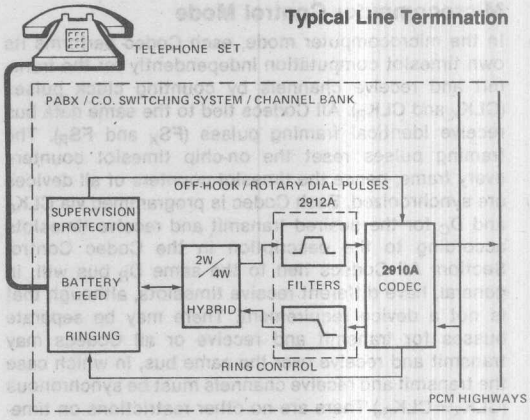
The Codec provides two major functions:

- Encoding and decoding of analog signals (voice and call progress tones)
- Encoding and decoding of the signaling and supervision information

On a non-signaling frame, the Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

For channel associated signaling, the Codec transmit side will encode the incoming analog signal as previously described and substitute the signal present on lead SIG_X for the least significant bit of the encoded PCM word. Similarly, on a receive signaling frame, the Codec will decode the 7 most significant bits according to the CCITT G733 recommendation and will output the least significant bit value on the SIG_R lead until the next signaling frame. Signaling frames on the send and receive sides are independent of each other, and are selected by a double-width frame sync pulse on the appropriate channel.

Typical Line Termination



The 2910A Codec is intended to be used on line and trunk terminations. The call progress tones (dial tone, busy tone, ring-back tone, re-order tone), and the pre-recorded announcements, can be sent through the voice-path; digital signaling (off hook and disconnect supervision, rotary dial pulses, ring control) is sent through the signaling path.

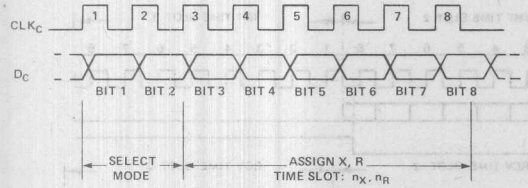
Circuitry is provided within the Codec to internally define the transmit and receive timeslots. In small systems this may eliminate the need for any external timeslot exchange; in large systems it provides one level of concentration. This feature can be bypassed and discrete timeslots sent to each Codec within a system.

In the power-down mode, most functions of the Codec are directly disabled to reduce power dissipation to a minimum.

CODEC OPERATION

Codec Control

The operation of the 2910A is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and Bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10), or whether the Codec should go into the standby, power-down mode (11). In the last case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the timeslot assignment, from 000000 (timeslot 1) to 111111 (timeslot 64). Bit 3 is the most significant bit and bit 8 the least significant bit and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit 3	4	5	6	7	8	Timeslot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
		•				•
		•				•
		•				•
		•				•
1	1	1	1	1	1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature permits dynamic allocation of timeslots for switching applications.

Microcomputer Control Mode

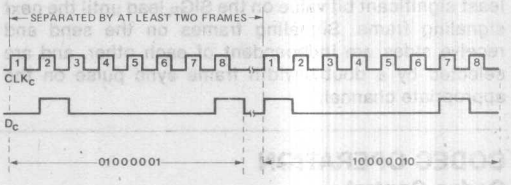
In the microcomputer mode, each Codec performs its own timeslot computation independently for the transmit and receive channels by counting clock pulses (CLK_X and CLK_R). All Codecs tied to the same data bus receive identical framing pulses (FS_X and FS_R). The framing pulses reset the on-chip timeslot counters every frame; hence the timeslot counters of all devices are synchronized. Each Codec is programmed via CLK_C and D_C for the desired transmit and receive timeslots according to the description in the Codec Control Section. All Codecs tied to the same D_R bus will, in general, have different receive timeslots, although that is not a device requirement. There may be separate busses for transmit and receive or all Codecs may transmit and receive over the same bus, in which case the transmit and receive channels must be synchronous ($CLK_X = CLK_R$.) There are no other restrictions on timeslot assignments; a device may have the same transmit and receive timeslot even if a single bus is used.

There are several requirements for using the CLK_C-D_C interface in the microcomputer mode.

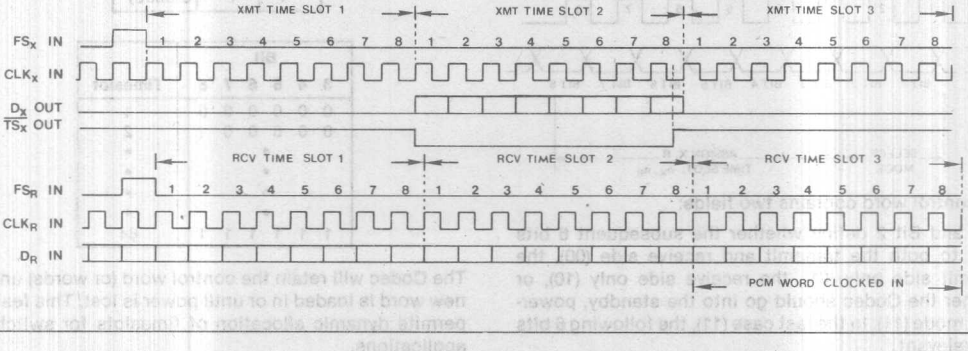
1. A complete timeslot assignment, consisting of eight negative transitions of CLK_C, must be made in less than one frame period. The assignment can overlap a framing pulse so long as all 8 control bits are clocked in within a total span of 125 μsec (for an 8 KHz frame rate). CLK_C must be left at a TTL low level when not assigning a timeslot.
2. A dead period of two frames must always be observed between successive timeslot assignments. The two frame delay is measured from the rising edge of the first CLK_C transition of the previous timeslot assigned.
3. When the device is in the power-down state a single control word will suffice to power-up the Codec and make a timeslot assignment. That is, the first assignment brings the device out of power-down and registers the timeslot information in the lower six bits of the control word.
4. Initialization sequence: The device contains an on-chip power-on clear function which guarantees that with proper sequencing of the supplies (V_{CC} or V_{DD} on last), the device will initialize with no timeslot assigned to either the transmit or receive channel. After a supply failure or whenever the supplies are applied, it is recommended that either power down assignment be made first, or the first timeslot assignment be a transmit timeslot or a transmit/receive timeslot. The consequence of making a receive timeslot assignment first, after supply application, is that the transmit channel will assume timeslot 1, potentially producing bus contention.
5. Transmit only/receive only operation is permitted provided that a power down assignment is made first. Otherwise, special circuits which use only one channel should be physically disconnected from the unused bus; this allows a timeslot to be made to an unused channel without consequence.
6. Both frame synchronizing pulses (FS_X, FS_R) must be active at all times after power on clear (after power supplies are turned on). This requirement must be met during powerdown and receive only or transmit only operation, as well as during normal transmit and receive operation.

Example of Microcomputer Control Mode:

The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for timeslot 2 and the receive side for timeslot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the timeslot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during timeslot 3.



In this example the Codec interface to the PCM highway then functions as shown below. (FS_X and FS_R may be asynchronous.)



Direct Control Mode

The direct mode of operation will be selected when the CLK_C pin is strapped to the +5 volt supply (V_{CC}). In this mode, the D_C pin is an active low chip select. In other words, when D_C is low, the device transmits and receives in the timeslots which follow the appropriate framing pulses. With D_C high the device is in the power down state. Even though CLK_C characteristics are simpler for the 2910A it will operate properly when plugged into a 2910 board.

Deactivation of a channel by removal of the appropriate framing pulse (FS_X or FS_R) is generally not permitted. Specifically, framing pulses must be applied for a minimum of two frames after a change in state of D_C in order for the D_C change to be internally sensed. In particular, when entering standby in the direct mode, framing pulses must be applied as usual for two frames after D_C is brought high. Thereafter, the framing pulses could, if desired, be removed until such time as the device is to be reactivated by the reapplication of framing pulses with D_C low.

The Codec will enter the direct mode within three frame times (375 μsec) as measured from the time the device power supplies settle to within the specified limits. This assumes that CLK_C is tied to V_{CC} and that all clocks are available at the time the supplies have settled.

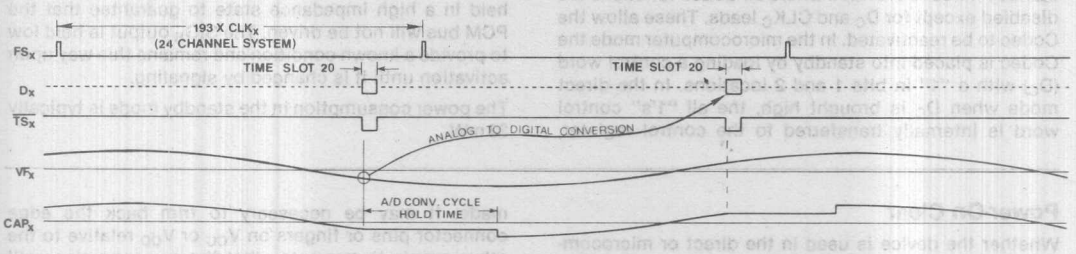
General Control Requirements

All bit and frame clocks should be applied whenever the device is active. In particular, an unused channel cannot be deactivated by removal of its associated frame or bit clock while the other channel of the same device remains active.

A single channel cannot be deactivated except by physical disconnection of the data lead (D_X or D_R) from the system data bus. A device (both transmit and receive channels) may be deactivated in either control mode by powering down the device. Both channels are always powered down together.

Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling and conversion is synchronized with the transmit timeslot. The PCM word is then output on the D_X lead at the proper timeslot occurrence of the following frame. The A/D converter saturates at approximately ±2.2 volts RMS (±3.1 volts peak).



Decoding

The PCM word is fetched by the D_R lead from the PCM highway at the proper timeslot occurrence. The decoded value is held on an internal sample and hold capacitor.

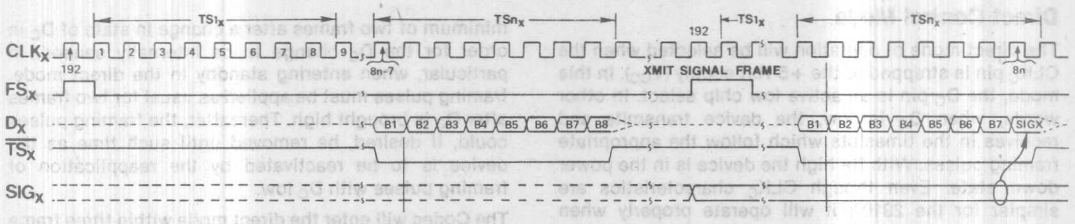
The buffered non-return to zero output signal on the VF_R lead has a dynamic range of approximately ±2.2 volts RMS (±3.1 volts peak).

Signaling

The duration of the FS_X and FS_R pulses defines whether a frame is an information frame or a signaling frame:

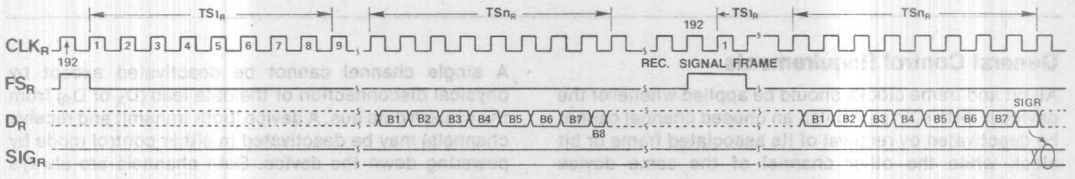
- A frame synchronization pulse which is a full clock period in duration (CLK_X period for FS_X, CLK_R period for FS_R) designates a non-signaling frame.
- A frame synchronization pulse which is two full clock periods in duration (two CLK_X periods for FS_X, two CLK_R periods for FS_R) designates a signaling frame.

On the encoding side, when the FS_X pulse is widened, the 8th bit of the PCM word will be replaced by the value on the SIG_X input at the time when the 8th bit is output on the D_X lead.



On the decoding side, when the FS_R pulse is widened, the 8th bit of the PCM word is detected and transmitted on the SIG_R lead. That output is latched until the next receiving signaling frame.

The remaining 7 bits are decoded according to the value given in the CCITT G733 recommendation. The SIG_R lead is reset to a TTL low level whenever the Codec is in the power-down state.



T1 Framing

The Codec will accept the standard D3/D4 framing format of 193 clock pulses per frame (equivalent to CLK_X, CLK_R of 1.544 Mb/sec). However, the 193rd bit may be blanked (equivalent to CLK_X, CLK_R of 1.536 Mb/sec) if desired.

Standby Mode — Power Down

To minimize power consumption and heat dissipation a standby mode is provided where all Codec functions are disabled except for D_C and CLK_C leads. These allow the Codec to be reactivated. In the microcomputer mode the Codec is placed into standby by loading a control word (D_C) with a "1" in bits 1 and 2 locations. In the direct mode when D_C is brought high, the all "1's" control word is internally transferred to the control register, invoking the standby condition.

While in the standby mode, the D_X output is actively held in a high impedance state to guarantee that the PCM bus will not be driven. The SIG_R output is held low to provide a known condition and remains this way upon activation until it is changed by signaling.

The power consumption in the standby mode is typically 33 mW.

Power-On Clear

Whether the device is used in the direct or microcomputer mode, an internal reset (power-on clear) is generated, forcing the device into the power down state, when power is supplied by any of the following methods. (1) Device power supplies are turned on in a system power-up situation where either V_{CC} or V_{DD} is applied last. (2) A large supply transient causes either of the two positive supplies to drop to less than approximately 2 volts. (3) A board containing Codecs is plugged into a "hot" system where V_{CC} or V_{DD} is the last contact made. It may be necessary to trim back the edge connector pins or fingers on V_{CC} or V_{DD} relative to the other supply to guarantee that the power-on clear will operate properly when a board is plugged into a "hot" system. Furthermore, the Codec will inhibit activity on $\overline{TS_X}$ and D_X during the application of power supplies.

The device is also tolerant of transients in the negative supply (V_{BB}) so long as V_{BB} remains more negative than −3.5 volts. V_{BB} transients which exceed this level should be detected and followed by a system reinitialization.

Precision Voltage Reference for the D/A Converter

The voltage reference is generated on the chip and is calibrated during the manufacturing process. The technique uses the difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature stable and bias stable reference voltage.

A gain setting op amp, programmed during manufacturing, "trims" the reference voltage source to the final precision voltage reference value provided to the D/A converter. The precision voltage reference determines the initial gain and dynamic range characteristics described in the A.C. Transmission Specification section.

μ-Law Conversion

μ-law represents a particular implementation of a piecewise linear approximation to a logarithmic compression curve which is:

$$F(x) = Sgn(x) \frac{\ln(1+\mu|x|)}{\ln(1+\mu)}, \quad 0 \leq |x| \leq 1$$

where x = input signal

Sgn(x) = sign of input signal

μ = 255 (defined by AT&T)

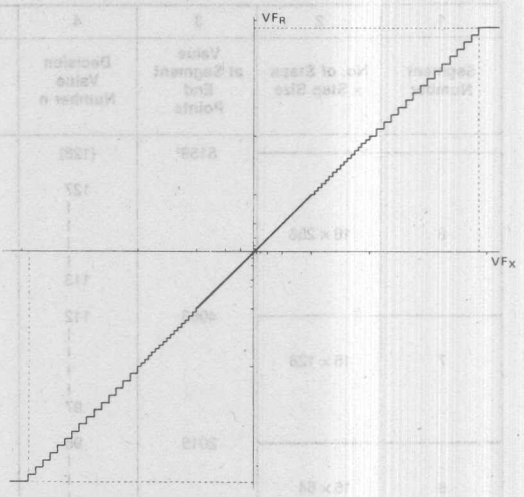
The 2910A μ = 255 law Codec uses a 15 segment approximation to the logarithmic law. Each segment consists of 16 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment the step size is constant except for the first step of the first segment of the encoder, as indicated in the attached table. The output levels are midway between the corresponding decision levels. The output levels y_n are related to the input levels x_n by the expression:

$$y_n = \frac{x_n + x_{n+1}}{2} \text{ for } 1 \leq n \leq 127$$

$$y_0 = x_0 = 0 \text{ for } n = 0$$

These relationships are implicit in the attached table.

CODEC TRANSFER CHARACTERISTIC



During signaling frames, a 7-bit transfer characteristic is implemented in the decoder. This characteristic is derived from the decoder values in the attached table by assuming a value of "1" for the LSB (8th bit) and shifting the decoder transfer characteristic one half-step away from the origin. For example, the maximum decoder output level for signaling frames has normalized value 7903, whereas it has value 8031 in normal (non-signaling) frames.

Theoretical μ-Law — Positive Input Values (for Negative Input Values, Invert Bit 1)

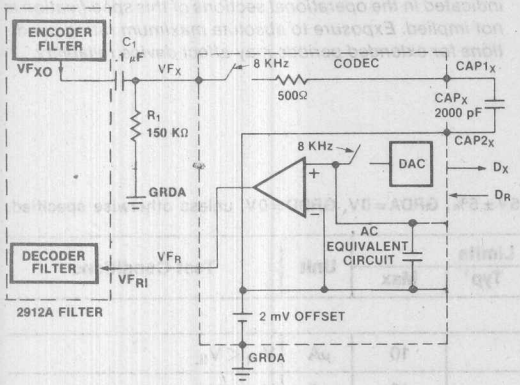
1	2	3	4	5	6	7	8
Segment Number	No. of Steps x Step Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n[1]	PCM Word[3] MSB Bit Number LSB 1 2 3 4 5 6 7 8	Normalized Value at Decoder Output y_n[4]	Decoder Output Value Number
		8159[5]	(128)	(8159)			
			127	7903	1 0 0 0 0 0 0 0	8031	127
8	16 × 256				(see Note 2)		
			113	4319	1 0 0 0 1 1 1 1	4191	112
		4063	112	4063			
7	16 × 128				(see Note 2)		
			97	2143	1 0 0 1 1 1 1 1	2079	96
		2015	96	2015			
6	16 × 64				(see Note 2)		
			81	1055	1 0 1 0 1 1 1 1	1023	80
		991	80	991			
5	16 × 32				(see Note 2)		
			65	511	1 0 1 1 1 1 1 1	495	64
		479	64	479			
4	16 × 16				(see Note 2)		
			49	239	1 1 0 0 1 1 1 1	231	48
		223	48	223			
3	16 × 8				(see Note 2)		
			33	103	1 1 0 1 1 1 1 1	99	32
		95	32	95			
2	16 × 4				(see Note 2)		
			17	35	1 1 1 0 1 1 1 1	33	16
		31	16	31			
	15 × 2				(see Note 2)		
			2	3			
1					1 1 1 1 1 1 1 0	2	1
↓	1 × 1		1	1	1 1 1 1 1 1 1 1		
			0	0		0	0

Notes:

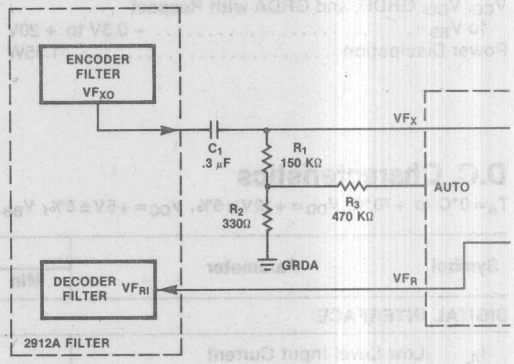
1. 8159 normalized value units correspond to the value of the on-chip voltage reference.
2. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 – n) expressed as a binary number.
3. The PCM word on the highways is the same as the one shown in column 6.
4. The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
5. x_{128} is a virtual decision value.

APPLICATIONS

Circuit Interface — Without External Auto Zero



Circuit Interface — With External Auto Zero



Holding Capacitor

For an 8KHz sampling system the transmit holding capacitor CAP_X should be 2000 pF ± 20%.

Auto Zero

The 2910A contains a transparent on-chip auto zero plus a device pin for implementing a sign-bit driven external auto zero feedback loop. The on-chip auto zero reduces the input offset voltage of the encoder (VF_X) to less than 3 mV. For most telephony applications, this input offset is perfectly acceptable, since it insures the encoder is biased in the lower 25% of the first segment.

Where lower input offset is required the external auto zero loop may be used to bias the encoder exactly at the zero crossing point. The consequence of the external auto zero loop, aside from extra components, is the addition of the dithering auto-zero signal to the input signal, resulting in slightly higher idle channel noise (approximately 2 dB) than when the external loop is not used. Consequently, where the application permits, it is recommended that the external auto zero loop not be used.

The circuit interface with auto zero drawing shows a possible connection between the VF_X and AUTO leads with the recommended values of $C_1 = 0.3\,\mu F$, $R_1 = 150\,K\Omega$, $R_2 = 330\,\Omega$, and $R_3 = 470\,K\Omega$.

Filters Interface

The filters may be interfaced as shown in the circuit interface diagrams. Note that the output pulse stream is of the non-return-to-zero type and hence requires the (sin x)/x correction provided by the 2912A filter.

D_X Buffering

For higher drive capability or increased system reliability it may be desirable that the D_X output of a group of Codecs be buffered from the system PCM bus with an external three-state or open collector buffers. A buffer can be enabled with the appropriate Codec generated $\overline{TS_X}$ signal or signals. $\overline{TS_X}$ signal may also be used to activate external zero code suppression logic, since the occurrence of an active state of any $\overline{TS_X}$ implies the existence of PCM voice bits (as opposed to transparent data bits) on the bus.

Absolute Maximum Ratings*

Temperature Under Bias −10°C to +80°C
Storage Temperature −65°C to +150°C
All Input or Output Voltages with Respect to V_{BB} −0.3V to +20V
V_{CC}, V_{DD}, GRDD, and GRDA with Respect to V_{BB} −0.3V to +20V
Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ[1]	Max		
DIGITAL INTERFACE						
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, $I_{OL} = 4.0$ mA SIG_R, $I_{OL} = 0.5$ mA $\overline{TS_X}$, $I_{OL} = 3.2$ mA, open drain PDN, $I_{OL} = 1.6$ mA, open drain
V_{OH}	Output High Voltage	2.4			V	D_X, $I_{OH} = 15$ mA SIG_R, $I_{OH} = 0.08$ mA
ANALOG INTERFACE						
Z_{AI}	Input Impedance when Sampling, VF_X	125	300	500	Ω	in series with CAP_X to GRDA, $-3.1V < V_{IN} < 3.1V$
Z_{AO}	Small Signal Output Impedance, VF_R	100	180	300	Ω	$-3.1V < V_{OUT} < 3.1V$
V_{OR}	Output Offset Voltage at VF_R			±50	mV	all "1s" code sent to D_R
V_{IX}	Input Offset Voltage at VF_X			±5	mV	VF_X voltage required to produce all "1s" code at D_X
V_{OL}	Output Low Voltage at AUTO		V_{BB}	(V_{BB} + 2)	V	400 KΩ to GRDA
V_{OH}	Output High Voltage at AUTO	(V_{CC} − 2)	V_{CC}		V	400 KΩ to GRDA
POWER DISSIPATION						
I_{DDO}	Standby Current		0.7	1.1	mA	Auto Output = Open clock frequency = 2.048 MHz
I_{CCO}	Standby Current		4	7.0	mA	
I_{BBO}	Standby Current		1	2.5	mA	
I_{DDI}	Operating Current		11	16	mA	
I_{CCI}	Operating Current		13	21	mA	
I_{BBI}	Operating Current		4	6.0	mA	

Notes:
1. Typical values are for $T_A = 25°C$ and nominal power supply values.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ[1]	Limits Max	Unit	Test Conditions
TRANSMISSION						
S/D	Signal/tone distortion ratio, C-Message weighted	36			dB	VF_X = 1.02 KHz, sinusoid -30 dBm0 ≤ VF_X ≤ 0 dBm0
	Half channel	30			dB	-40 dBm0 ≤ VF_X < -30 dBm0
	(See Figure 1)	27			dB	-45 dBm0 ≤ VF_X < -40 dBm0
ΔG						VF_X = 1.02 KHz, sinusoid
	Gain tracking deviation		±.25	±.30	dB	-37 dBm0 ≤ VF_X ≤ +3 dBm0
	Half channel[2]		±.60	±.70	dB	-50 dBm0 ≤ VF_X < -37 dBm0
	Reference level 0 dBm0		±1.5	±1.8	dB	-55 dBm0 ≤ VF_X < -50 dBm0
ΔG_V	ΔG Variation with supplies		±.0002	±.0004	dB/mV	-37 dBm0 ≤ VF_X ≤ +3 dBm0
	Half channel		±.0004	±.0008	dB/mV	-50 dBm0 ≤ VF_X < -37 dBm0
ΔG_T	ΔG Variation with temperature		±.001	±.002	dB/°C	-37 dBm0 ≤ VF_X ≤ +3 dBm0
	Half channel		±.002	±.005	dB/°C	-50 dBm0 ≤ VF_X < -37 dBm0
N_{IC1}	Idle channel noise, C-Message weighted		2	7	dBrnc0	no signaling[3]
N_{IC2}	Idle channel noise, C-Message weighted		10	13	dBrnc0	with 6th and 12th frame signaling[3]
N_{IC3}	Idle channel noise, C-Message weighted		14	18	dBrnc0	with 1KHz sign bit toggle
HD	Harmonic distortion (2nd or 3rd)		-48	-44	dB	VF_X = 1.02 KHz, 0 dBm0; measured at decoder output VF_R
IMD	Intermodulation distortion					4-tone stimulus in accordance with BSTR PUB 41009
	2nd Order			-45	dB	
	3rd Order			-55	dB	

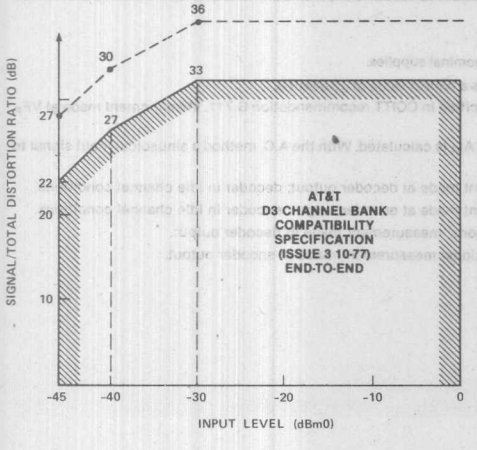


Figure 1. Signal/Total Distortion Ratio (Half-Channel)

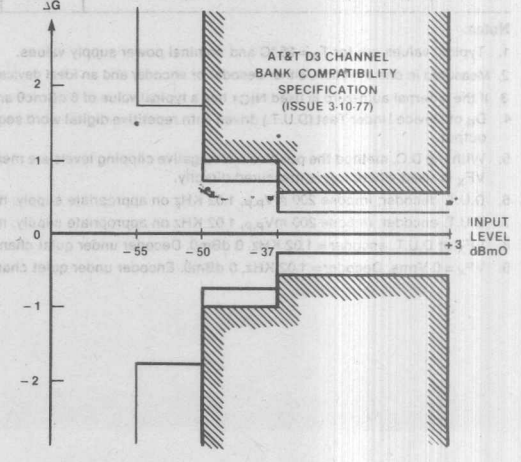


Figure 2. Gain Tracking Deviation (△G) (Half-Channel)

A.C. Characteristics (continued)

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ[1]	Max		
GAIN AND DYNAMIC RANGE						
DmW	Digital Milliwatt Response	5.53	5.63	5.73	dBm	23°C, nominal supplies[4]
DmW_T	DmW_O Variation with Temperature		−0.001	−0.002	dB/°C	relative to 23°C[4]
DmW_S	DmW_O Variation with Supplies			±0.07	dB	supplies ±5%[4]
A_{IR}	Input Dynamic Range	2.17	2.20	2.23	V_{RMS}	using D.C. and A.C. tests[5] 23°C, nominal supplies
A_{IRT}	Input Dynamic Range with Temperature			−0.5	mV_{RMS}/°C	relative to 23°C
A_{IRS}	Input Dynamic Range with Supplies			±18	mV_{RMS}	supplies ±5%
A_{OR}	Output Dynamic Range, VF_R	2.13	2.16	2.19	V_{RMS}	23°C, nominal supplies
A_{ORT}	A_{OR} Variation with Temperature			−0.5	mV_{RMS}/°C	relative to 23°C
A_{ORS}	A_{OR} Variation with Supplies			±18	mV_{RMS}	supplies ±5%
SUPPLY REJECTION AND CROSSTALK						
$PSRR_1$	V_{DD} Power Supply Rejection Ratio	45			dB	decoder alone[6]
$PSRR_2$	V_{BB} Power Supply Rejection Ratio	35			dB	decoder alone[6]
$PSRR_3$	V_{CC} Power Supply Rejection Ratio	50			dB	decoder alone[6]
$PSRR_4$	V_{DD} Power Supply Rejection Ratio	50			dB	encoder alone[7]
$PSRR_5$	V_{BB} Power Supply Rejection Ratio	45			dB	encoder alone[7]
$PSRR_6$	V_{CC} Power Supply Rejection Ratio	50			dB	encoder alone[7]
CT_R	Crosstalk Isolation, Receive Side	75	80		dB	see Note 8
CT_T	Crosstalk Isolation, Transmit Side	75	80		dB	see Note 9
CAPX	Input Sample and Hold Capacitor	1600	2000	2400	pF	

Notes:

1. Typical values are for $T_A = 25°C$ and nominal power supply values.
2. Measured in one direction, either decoder or encoder and an ideal device, at 23°C, nominal supplies.
3. If the external auto-zero is used N_{IC1} has a typical value of 8 dBrnc0 and N_{IC2} has a typical value of 13 dBrnc0.
4. D_R of Device Under Test (D.U.T.) driven with repetitive digital word sequence specified in CCITT recommendation G.711. Measurement made at VF_R output.
5. With the D.C. method the positive and negative clipping levels are measured and A_{IR} is calculated. With the A.C. method a sinusoidal input signal to VF_X is used where A_{IR} is measured directly.
6. D.U.T. decoder; impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at decoder output; decoder in idle channel conditions.
7. D.U.T. encoder; impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at encoder output; encoder in idle channel conditions.
8. VF_X of D.U.T. encoder = 1.02 KHz, 0 dBm0. Decoder under quiet channel conditions; measurement made at decoder output.
9. $VF_X = 0$ Vrms. Decoder = 1.02 KHz, 0 dBm0. Encoder under quiet channel conditions; measurement made at encoder output.

A.C. Characteristics — Timing Specification (1)

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Max	Units	Comments
CLOCK SECTION					
t_{CY}	Clock Period	485		ns	CLK_X, CLK_R (2.048 MHz systems), CLK_C
t_r, t_f	Clock Rise and Fall Time	0	30	ns	CLK_X, CLK_R, CLK_C
t_{CLK}	Clock Pulse Width	215		ns	CLK_X, CLK_R, CLK_C
t_{CDC}	Clock Duty Cycle ($t_{CLK} \div t_{CY}$)	45	55	%	CLK_X, CLK_R
TRANSMIT SECTION					
t_{VFX}	Analog Input Conversion	20		timeslot	from leading edge of transmit timeslot[2]
t_{DZX}	Data Enabled on TS Entry	50	180	ns	$0 < C_{LOAD} < 100\,pF$
t_{DHX}	Data Hold Time	80	230	ns	$0 < C_{LOAD} < 100\,pF$
t_{HZX}	Data Float on TS Exit	75	245	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	30	220	ns	$0 < C_{LOAD} < 100\,pF$
t_{SOFF}	Timeslot X to Disable	70	225	ns	$C_{LOAD} = 0$
t_{SS}	Signal Setup Time	0		ns	relative to bit 7 falling edge
t_{SH}	Signal Hold Time	100		ns	relative to bit 8 falling edge
t_{FSD}	Frame Sync Delay	15	150	ns	
RECEIVE AND CONTROL SECTIONS					
t_{VFR}	Analog Output Update	9 1/16	9 1/16	timeslot	from leading edge of the channel timeslot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	60		ns	
t_{SIGR}	SIG_R Update		1	μs	from trailing edge of the channel timeslot
t_{FSD}	Frame Sync Delay	15	150	ns	
t_{DSC}	Control Data Setup	115		ns	Microcomputer mode only
t_{DHC}	Control Data Hold	115		ns	Microcomputer mode only

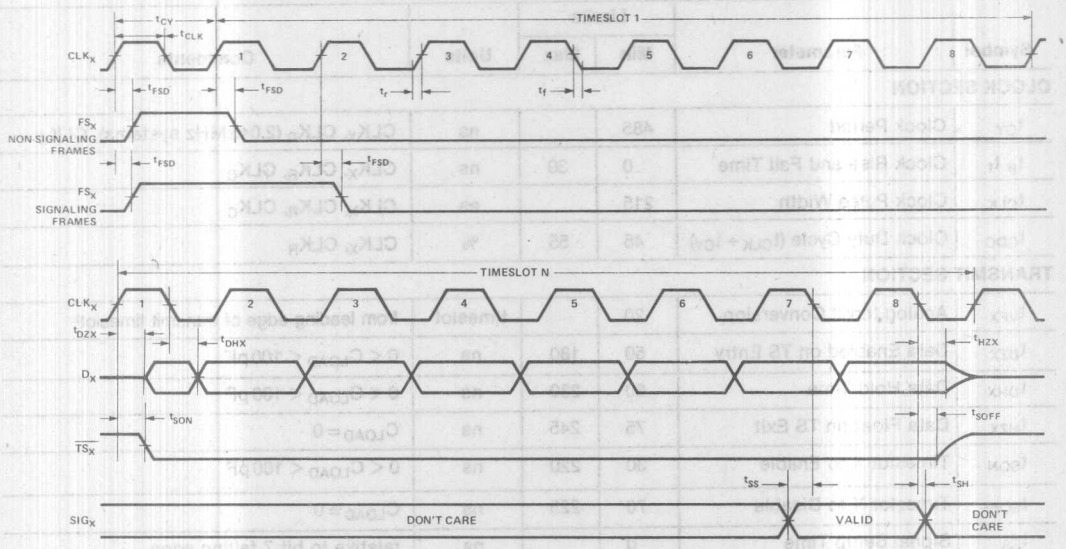
Notes:

1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF} which reference to high impedance state.

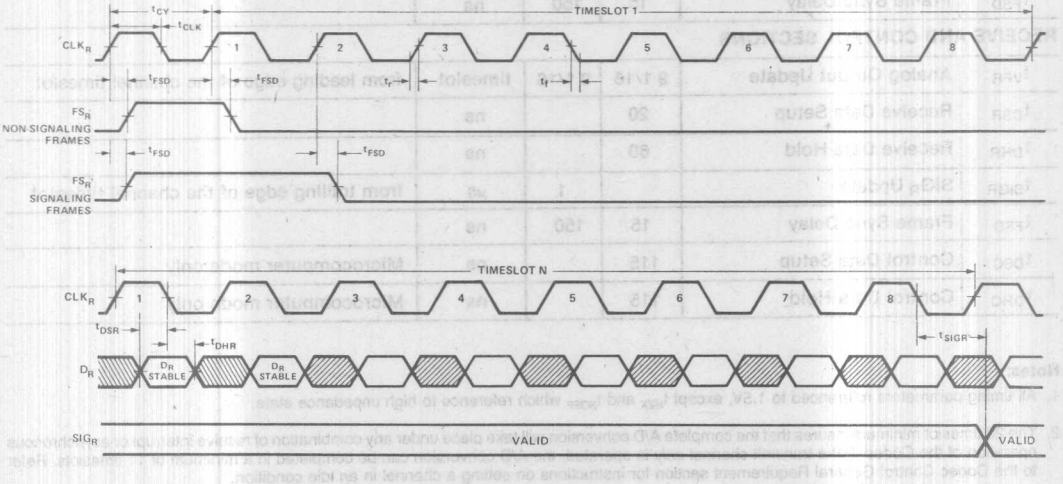
2. The 20 timeslot minimum insures that the complete A/D conversion will take place under any combination of receive interrupt or asynchronous operation of the Codec. If the transmit channel *only* is operated, the A/D conversion can be completed in a minimum of 11 timeslots. Refer to the Codec Control General Requirement section for instructions on setting a channel in an idle condition.

TIMING WAVEFORMS[1]

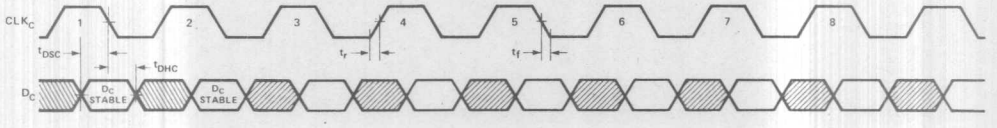
TRANSMIT TIMING



RECEIVE TIMING



CONTROL TIMING



Notes: 1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF} which reference a high impedance state.

2911A-1
PCM CODEC — A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible, Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots Are Used**
- **66 dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **±5% Power Supplies: +12V, +5V, −5V**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33 mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel® 2911A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

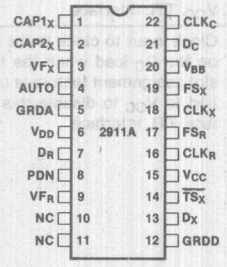
The primary applications are in telephone systems:

- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

The wide dynamic range of the 2911A (66 dB) and the minimal conversion time (80 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Secure Communications Systems
- Telemetry
- Signal Processing Systems

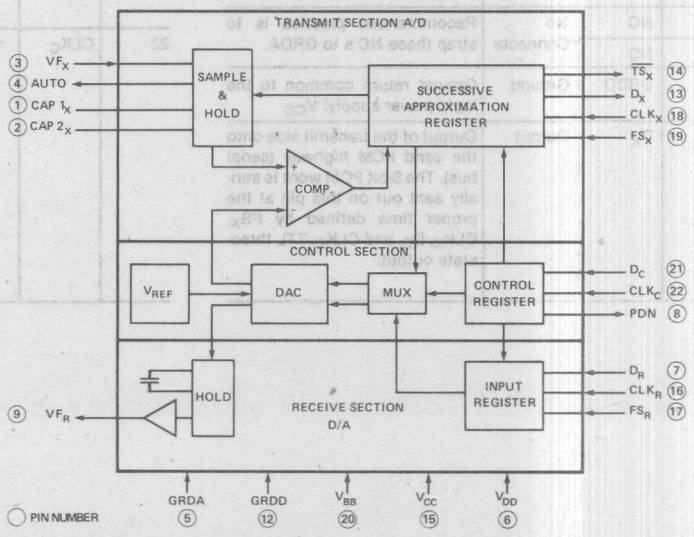
PIN CONFIGURATION



PIN NAMES

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C	Digital Input
D_X, $\overline{TS_X}$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

BLOCK DIAGRAM



PIN DESCRIPTION

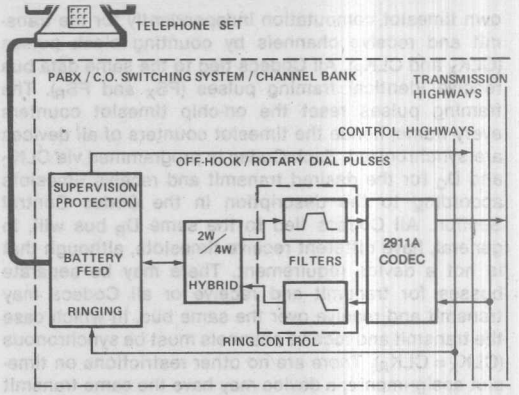
Pin No.	Symbol	Function	Description
1	$CAP1_X$	Hold	Connections for the transmit holding capacitor. Refer to Applications section.
2	$CAP2_X$		
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for negative, −5V for positive values). Refer to the Codec Applications section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
6	V_{DD}	Power	+12V ± 5%; referenced to GRDA.
7	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8 bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
8	PDN	Output	Active high when the Codec is in the power down state. Open drain output.
9	VF_R	Output	Analog Output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions.
10	NC	No Connects	Recommended practice is to strap these NC's to GRDA.
11	NC		
12	GRDD	Ground	Ground return common to the logic power supply; V_{CC}.
13	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
14	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Timeslot information used for diagnostic purposes and also to gate the data on the D_X lead.) Open drain output.
15	V_{CC}	Power	+5V ± 5%, referenced to GRDD.
16	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL compatible.
17	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Resets the on-chip timeslot counter for the receive side. Maximum repetition rate 12 KHz. TTL interface.
18	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
19	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Resets the on-chip timeslot counter for the transmit side. Maximum repetition rate 12 KHz. TTL interface.
20	V_{BB}	Power	−5V ± 5%, referenced to GRDA.
21	D_C	Input	Data input to program the Codec for the chosen mode of operation. Becomes an active low chip select when CLK_C is tied to V_{CC}. TTL interface.
22	CLK_C	Input	Clock input to clock in the data on the D_C lead when the timeslot assignment feature is used; tied to V_{CC} to disable this feature. TTL interface.

The 2911A PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. The Codec is intended to be used on line and trunk terminations.

In a typical telephone system the Codec is located between the PCM highways and the channel filters.

The Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

Circuitry is provided within the Codec to internally define the transmit and receive timeslots. In small systems this may eliminate the need for any external timeslot exchange; in large systems it provides one level of concentration. This feature can be bypassed and discrete timeslots sent to each Codec within a system.

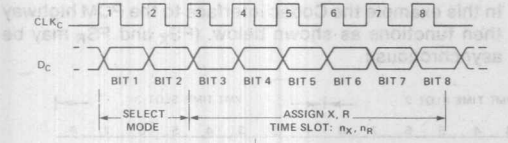


In the power-down mode, most functions of the Codec are directly disabled to reduce power dissipation to a minimum.

CODEC OPERATION

Codec Control

The operation of the 2911A is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and Bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10), or whether the Codec should go into the standby, power-down mode (11). In the last case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the timeslot assignment, from 000000 (timeslot 1) to 111111 (timeslot 64). Bit 3 is the most significant bit and bit 8 the least significant bit and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit						
3	4	5	6	7	8	Time-Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
		•				•
		•				•
		•				•
		•				•
1	1	1	1	1	1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature permits dynamic allocation of timeslots for switching applications.

Microcomputer Control Mode

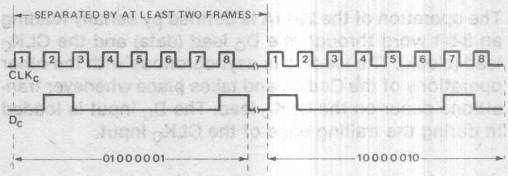
In the microcomputer mode, each Codec performs its own timeslot computation independently for the transmit and receive channels by counting clock pulses (CLK_X and CLK_R). All Codecs tied to the same data bus receive identical framing pulses (FS_X and FS_R). The framing pulses reset the on-chip timeslot counters every frame; hence the timeslot counters of all devices are synchronized. Each Codec is programmed via CLK_C and D_C for the desired transmit and receive timeslots according to the description in the Codec Control Section. All Codecs tied to the same D_R bus will, in general, have different receive timeslots, although that is not a device requirement. There may be separate busses for transmit and receive or all Codecs may transmit and receive over the same bus, in which case the transmit and receive channels must be synchronous ($CLK_X = CLK_R$). There are no other restrictions on timeslot assignments; a device may have the same transmit and receive timeslot even if a single bus is used.

There are several requirements for using the CLK_C-D_C interface in the microcomputer mode.

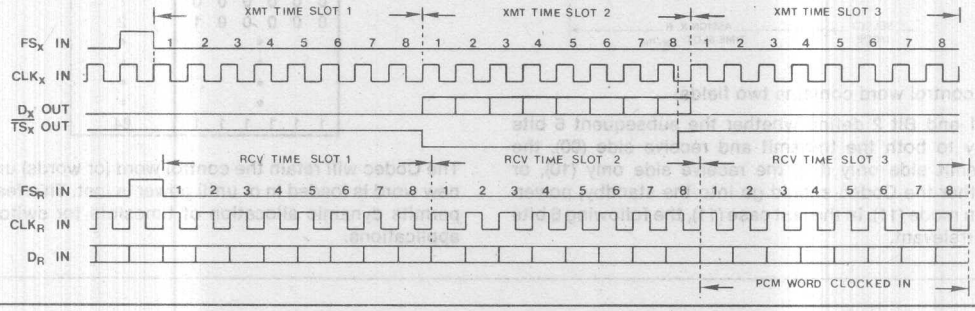
1. A complete timeslot assignment, consisting of eight negative transitions of CLK_C, must be made in less than one frame period. The assignment can overlap a framing pulse so long as all 8 control bits are clocked in within a total span of 125 μsec (for an 8 KHz frame rate). CLK_C must be left at a TTL low level when not assigning a timeslot.
2. A dead period of two frames must always be observed between successive timeslot assignments. The two frame delay is measured from the rising edge of the first CLK_C transition of the previous timeslot assigned.
3. When the device is in the power-down state a single control word will suffice to power-up the Codec and make a timeslot assignment. That is, the first assignment brings the device out of power-down and registers the timeslot information in the lower six bits of the control word.
4. Initialization sequence: The device contains an on-chip power-on clear function which guarantees that with proper sequencing of the supplies (V_{CC} or V_{DD} on last), the device will initialize with no timeslot assigned to either the transmit or receive channel. After a supply failure or whenever the supplies are applied, it is recommended that either power down assignment be made first, or the first timeslot assignment be a transmit timeslot or a transmit/receive timeslot. The consequence of making a receive timeslot assignment first, after supply application, is that the transmit channel will assume timeslot 1, potentially producing bus contention.
5. Transmit only/receive only operation is permitted provided that a power down assignment is made first. Otherwise, special circuits which use only one channel should be physically disconnected from the unused bus; this allows a timeslot to be made to an unused channel without consequence.
6. Both frame synchronizing pulses (FS_X, FS_R) must be active at all times after power on clear (after power supplies are turned on). This requirement must be met during powerdown and receive only or transmit only operation, as well as during normal transmit and receive operation.

Example of Microcomputer Control Mode:

The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for timeslot 2 and the receive side for timeslot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the timeslot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during timeslot 3.



In this example the Codec interface to the PCM highway then functions as shown below. (FS_X and FS_R may be asynchronous.)



Direct Control Mode

The direct mode of operation will be selected when the CLK_C pin is strapped to the +5 volt supply (V_{CC}). In this mode, the D_C pin is an active low chip select. In other words, when D_C is low, the device transmits and receives in the timeslots which follow the appropriate framing pulses. With D_C high the device is in the power down state. Even though CLK_C characteristics are simpler for the 2911A it will operate properly when plugged into a 2911 board.

Deactivation of a channel by removal of the appropriate framing pulse (FS_X or FS_R) is not permitted.

Specifically, framing pulses must be applied for a minimum of two frames after a change in state of D_C in order for the D_C change to be internally sensed. In particular, when entering standby in the direct mode, framing pulses must be applied as usual for two frames after D_C is brought high. Thereafter, the framing pulses could, if desired, be removed until such time as the device is to be reactivated by the reapplication of framing pulses with D_C low.

The Codec will enter the direct mode within three frame times (375 μsec) as measured from the time the device power supplies settle to within the specified limits. This assumes that CLK_C is tied to V_{CC} and that all clocks are available at the time the supplies have settled.

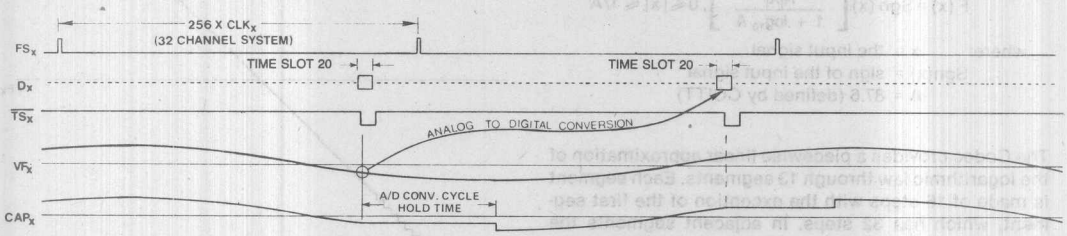
General Control Requirements

All bit and frame clocks should be applied whenever the device is active. In particular, an unused channel cannot be deactivated by removal of its associated frame or bit clock while the other channel of the same device remains active.

A single channel cannot be deactivated except by physical disconnection of the data lead (D_X or D_R) from the system data bus. A device (both transmit and receive channels) may be deactivated in either control mode by powering down the device. Both channels are always powered down together.

Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling and conversion is synchronized with the transmit timeslot. The PCM word is then output on the D_X lead at the proper timeslot occurrence of the following frame. The A/D converter saturates at approximately ±2.2 volts RMS (±3.1 volts peak).



Decoding

The PCM word is fetched by the D_R lead from the PCM highway at the proper timeslot occurrence. The decoded value is held on an internal sample and hold capacitor.

The buffered non-return to zero output signal on the VF_R lead has a dynamic range of ±2.2 volts RMS (±3.1 volts peak).

Standby Mode — Power Down

To minimize power consumption and heat dissipation a standby mode is provided where all Codec functions are disabled except for D_C and CLK_C leads. These allow the Codec to be reactivated. In the microcomputer mode the Codec is placed into standby by loading a control word (D_C) with a "1" in bits 1 and 2 locations. In the direct mode when D_C is brought high, the all "1's" control word is internally transferred to the control register, invoking the standby condition.

While in the standby mode, the D_X output is actively held in a high impedance state to guarantee that the PCM bus will not be driven.

The power consumption in the standby mode is typically 33 mW.

Power-On Clear

Whether the device is used in the direct or microcomputer mode, an internal reset (power-on clear) is generated, forcing the device into the power down state, when power is supplied by any of the following methods. (1) Device power supplies are turned on in a system power-up situation where either V_{CC} or V_{DD} is applied last. (2) A large supply transient causes either of the two positive supplies to drop to approximately 2 volts. (3) A board containing Codecs is plugged into a

"hot" system where V_{CC} or V_{DD} is the last contact made. It may be necessary to trim back the edge connector pins or fingers on V_{CC} or V_{DD} relative to the other supply to guarantee that the power-on clear will operate properly when a board is plugged into a "hot" system. Furthermore, the Codec will inhibit activity on $\overline{TS}_X$ and D_X during the application of power supplies.

The device is also tolerant of transients in the negative supply (V_{BB}) so long as V_{BB} remains more negative than −3.5 volts. V_{BB} transients which exceed this level should be detected and followed by a system reinitialization.

Precision Voltage Reference for the D/A Converter

The voltage reference is generated on the chip and is calibrated during the manufacturing process. The technique uses the difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature stable and bias stable reference voltage.

A gain setting op amp, programmed during manufacturing, "trims" the reference voltage source to the final precision voltage reference value provided to the D/A converter. The precision voltage reference determines the initial gain and dynamic range characteristics described in the A.C. Transmission Specification section.

CONVERSION LAW

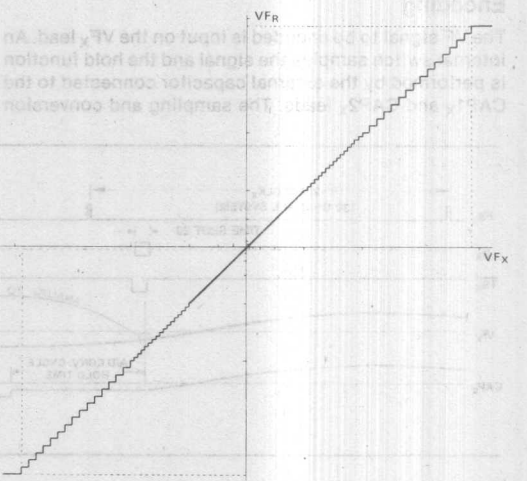
The conversion law is commonly referred to as the A Law.

$$F(x) = \mathrm{Sgn}(x)\left[\frac{1 + \log_{10}(A|X|)}{1 + \log_{10} A}\right], \quad 1/A \leq |x| \leq 1$$

$$F(x) = \mathrm{Sgn}(x)\left[\frac{A|X|}{1 + \log_{10} A}\right], \quad 0 \leq |x| \leq 1/A$$

where: x = the input signal
Sgn(x) = sign of the input signal
A = 87.6 (defined by CCITT)

CODEC TRANSFER CHARACTERISTIC



The Codec provides a piecewise linear approximation of the logarithmic law through 13 segments. Each segment is made of 16 steps with the exception of the first segment, which has 32 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment, the step size is constant.

The output levels are midway between the corresponding decision levels. The output levels y_n are related to the input levels x_n by the expression:

$$y_n = \frac{x_{n-1} + x_n}{2}, \quad 0 < n \leq 128$$

1	2	3	4	5	6	7	8
Segment Number	No. of Steps x Step Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n[1]	PCM Word[4] Bit Number 1 2 3 4 5 6 7 8	Normalized Value at Decoder Output y_n[5]	Decoder Output Value Number
		4096[3]	(128)	(4096)			
					1 1 1 1 1 1 1 1	4032	128
			127	3968			
7	16 × 128				(see Note 2)		
			113	2176			
					1 1 1 1 0 0 0 0	2112	113
		2048	112	2048			
6	16 × 64				(see Note 2)		
			97	1088			
					1 1 1 0 0 0 0 0	1056	97
		1024	96	1024			
5	16 × 32				(see Note 2)		
			81	544			
					1 1 0 1 0 0 0 0	528	81
		512	80	512			
4	16 × 16				(see Note 2)		
			65	272			
					1 1 0 0 0 0 0 0	264	65
		256	64	256			
3	16 × 8				(see Note 2)		
			49	136			
					1 0 1 1 0 0 0 0	132	49
		128	48	128			
2	16 × 4				(see Note 2)		
			33	68			
					1 0 1 0 0 0 0 0	66	33
		64	32	64			
1	32 × 2				(see Note 2)		
			1	2			
					1 0 0 0 0 0 0 0	1	1
			0	0			

Notes:

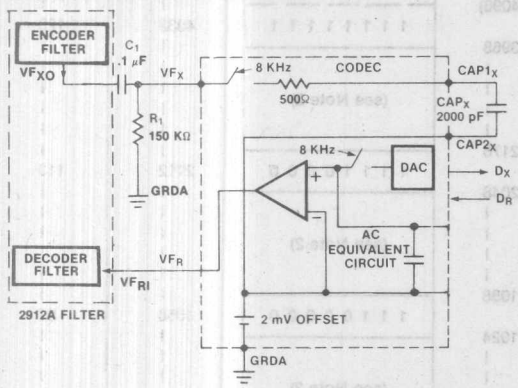
1. 4096 normalized value units correspond to the value of the on-chip voltage reference.
2. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (128 + n) expressed as a binary number.
3. X_{128} is a virtual decision value.
4. The PCM word on the highways is the same as the one shown in column 6, with the even order bits inverted. The 2911A provides for the inversion of the even order bits on both the send and receive sections.
5. The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.

APPLICATIONS

Holding Capacitor

For an 8KHz sampling system the transmit holding capacitor CAP_X should be 2000pF ± 20%.

Circuit Interface — Without External Auto Zero



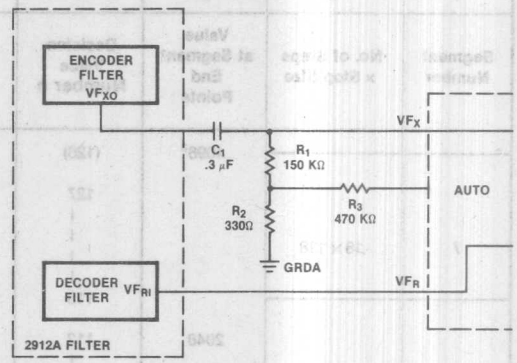
Filters Interface

The filters may be interfaced as shown in the circuit interface diagrams. Note that the output pulse stream is of the non-return-to-zero type and hence requires the (sin x)/x correction provided by the 2912A filter.

D_X Buffering

For higher drive capability or increased system reliability it may be desirable that the D_X output of a group of Codecs be buffered from the system PCM bus with an external three-state or open collector buffers. A buffer can be enabled with the appropriate Codec generated $\overline{TS}_X$ signal or signals. $\overline{TS}_X$ signal may also be used to activate external zero code suppression logic, since the occurrence of an active state of any $\overline{TS}_X$ implies the existence of PCM voice bits (as opposed to transparent data bits) on the bus.

Circuit Interface — With External Auto Zero



Auto Zero

The 2911A contains a transparent on-chip auto zero plus a device pin for implementing a sign-bit driven external auto zero feedback loop. The on-chip auto zero reduces the input offset voltage of the encoder (VF_X) to less than 3mV. For most telephony applications, this input offset is perfectly acceptable, since it insures the encoder is biased in the lower 25% of the first segment.

Where lower input offset is required the external auto zero loop may be used to bias the encoder exactly at the zero crossing point. The consequence of the external auto zero loop, aside from extra components, is the addition of the dithering auto-zero signal to the input signal, resulting in slightly higher idle channel noise (approximately 2dB) than when the external loop is not used. Consequently, where the application permits, it is recommended that the external auto zero loop not be used.

The circuit interface with external auto zero drawing shows a possible connection between VF_X and AUTO leads with the recommended values of $C_1 = 0.3\,\mu F$, $R_1 = 150\,K\Omega$, $R_2 = 330\,\Omega$, and $R_3 = 470\,K\Omega$.

Absolute Maximum Ratings*

Temperature Under Bias −10°C to +80°C
Storage Temperature −65°C to +150°C
All Input or Output Voltages with Respect to V_{BB} −0.3V to +20V
V_{CC}, V_{DD}, GRDA, and GRDA with Respect to V_{BB} −0.3V to +20V
Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ[1]	Limits Max	Unit	Test Conditions
DIGITAL INTERFACE						
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, $I_{OL} = 4.0$ mA $\overline{TS_X}$, $I_{OL} = 3.2$ mA, open drain PDN, $I_{OL} = 1.6$ mA, open drain
V_{OH}	Output High Voltage	2.4			V	D_X, $I_{OH} = 15$ mA
ANALOG INTERFACE						
Z_{AI}	Input Impedance when Sampling, VF_X	125	300	500	Ω	In series with CAP_X to GRDA, $-3.1V < V_{IN} < 3.1V$
Z_{AO}	Small Signal Output Impedance, VF_R	100	180	300	Ω	$-3.1V < V_{OUT} < 3.1V$
V_{OR}	Output Offset Voltage at VF_R	−50		50	mV	Minimum code to D_R
V_{IX}	Input Offset Voltage at VF_X	−5		5	mV	Minimum positive code produced at D_X
V_{OL}	Output Low Voltage at AUTO		V_{BB}	$(V_{BB} + 2)$	V	400 KΩ to GRDA
V_{OH}	Output High Voltage at AUTO	$(V_{CC} - 2)$	V_{CC}		V	400 KΩ to GRDA
POWER DISSIPATION						
I_{DDO}	Standby Current		0.7	1.1	mA	Auto Output = Open clock frequency = 2.048 MHz
I_{CCO}	Standby Current		4.0	7.0	mA	
I_{BBO}	Standby Current		1.0	2.5	mA	
I_{DDI}	Operating Current		11	16	mA	
I_{CCI}	Operating Current		13	21	mA	
I_{BBI}	Operating Current		4.0	6.0	mA	

Notes:
1. Typical values are for $T_A = 25°C$ and nominal power supply values.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits Min	Typ[1]	Max	Unit	Test Conditions
TRANSMISSION						
S/D	Signal to total distortion ratio. CCITT G.712 Method 2 (Half channel)	37			dB	Signal level 0 dBm0 to -30 dBm0
		31			dB	Signal level to -40 dBm0
		26			dB	Signal level to -45 dBm0
ΔG	2911A Gain tracking deviation		±.25	±.30	dB	VF_X = 1.02 KHz, sinusoid -40 dBm0 ≤ VF_X ≤ +3 dBm0
	Half channel[3]		±.60	±.70	dB	-50 dBm0 ≤ VF_X < -40 dBm0
	Reference level -10 dBm0		±1.5	±1.8	dB	-55 dBm0 ≤ VF_X < -50 dBm0
ΔG_V	ΔG Variation with supplies		±.0002	±.0004	dB/mV	-40 dBm0 ≤ VF_X ≤ +3 dBm0
	Half channel		±.0004	±.0008	dB/mV	-50 dBm0 ≤ VF_X < -40 dBm0
ΔG_T	ΔG Variation with temperature		±.001	±.002	dB/°C	-40 dBm0 ≤ VF_X ≤ +3 dBm0
	Half channel		±.002	±.005	dB/°C	-50 dBm0 ≤ VF_X < -40 dBm0
N_{IC}	Idle channel noise		-85	-78	dBm0p	Quiet code, see note 2
HD	Harmonic Distortion (2nd or 3rd)		-48	-44	dB	VF_X = 1.02 KHz, 0 dBm0; measured at decoder output VF_R
	Intermodulation Distortion					
IMD_1	G.712 (8.1)			-45	dB	CCITT G.712
IMD_2	G.712 (8.2)			-50	dBm0	Two tone method

Notes:
1. Typical values are for T_A = 25° C and nominal power supply values.
2. If the external auto zero is used N_{IC} has a typical value of -76 dBm0.
3. Tested and guaranteed at 23° C, nominal supplies.

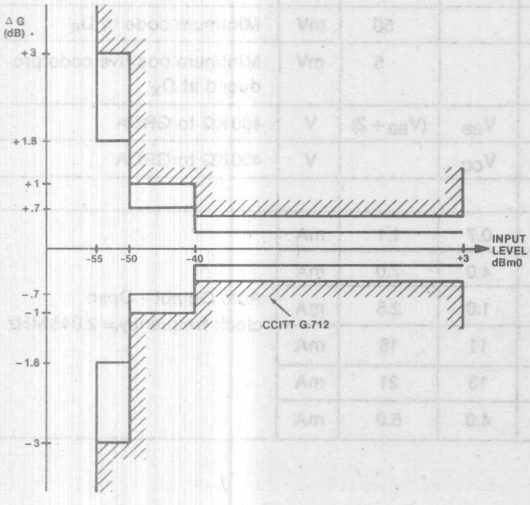


Figure 1. Tracking Deviation (ΔG) (Half Channel)

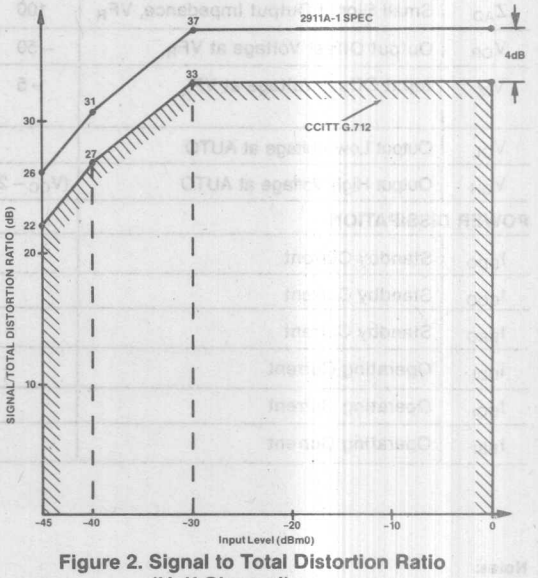


Figure 2. Signal to Total Distortion Ratio (Half Channel)

A.C. Characteristics (continued)

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ[1]	Max		
GAIN AND DYNAMIC RANGE						
DmW	Digital Milliwatt Response	5.58	5.66	5.78	dBm	23°C, nominal supplies[4]
DmW_T	DmW_O Variation with Temperature		−0.001	−0.002	dB/°C	Relative to 23°C[4]
DmW_S	DmW_O Variation with Supplies			±0.07	dB	Supplies ±5%[4]
A_{IR}	Input Dynamic Range	2.183	2.213	2.243	V_{RMS}	Using D.C. and A.C. tests[5] 23°C, nominal supplies
A_{IRT}	Input Dynamic Range vs Temperature			−0.5	mV_{RMS}/°C	Relative to 23°C
A_{IRS}	Input Dynamic Range vs Supplies			±18	mV_{RMS}	Supplies ±5%
A_{OR}	Output Dynamic Range, VF_R	2.14	2.17	2.20	V_{RMS}	23°C, nominal supplies
A_{ORT}	A_{OR} Variation with Temperature			−0.5	mV_{RMS}/°C	Relative to 23°C
A_{ORS}	A_{OR} Variation with Supplies			±18	mV_{RMS}	Supplies ±5%
SUPPLY REJECTION AND CROSSTALK						
$PSRR_1$	V_{DD} Power Supply Rejection Ratio	45			dB	decoder alone[6]
$PSRR_2$	V_{BB} Power Supply Rejection Ratio	35			dB	decoder alone[6]
$PSRR_3$	V_{CC} Power Supply Rejection Ratio	50			dB	decoder alone[6]
$PSRR_4$	V_{DD} Power Supply Rejection Ratio	50			dB	encoder alone[7]
$PSRR_5$	V_{BB} Power Supply Rejection Ratio	45			dB	encoder alone[7]
$PSRR_6$	V_{CC} Power Supply Rejection Ratio	50			dB	encoder alone[7]
CT_R	Crosstalk Isolation, Receive Side	75	80		dB	See Note 8
CT_T	Crosstalk Isolation, Transmit Side	75	80		dB	See Note 9
CAPX	Input Sample and Hold Capacitor	1600	2000	2400	pF	

Notes:

4. D_R of Device Under Test (D.U.T.) driven with repetitive digital word sequence specified in CCITT recommendation G.711. Measurement made at VF_R output.
5. With the D.C. method the positive and negative clipping levels are measured and A_{IR} is calculated. With the A.C. method a sinusoidal input signal to VF_X is used where A_{IR} is measured directly.
6. D.U.T. decoder; impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at decoder output; decoder in idle channel conditions.
7. D.U.T. encoder, impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at encoder output; encoder in idle channel conditions.
8. VF_X of D.U.T. encoder = 1.02 KHz, 0 dBm0. Decoder under quiet channel conditions; measurement made at decoder output.
9. VF_X = 0 Vrms. Decoder = 1.02 KHz, 0 dBm0. Encoder under quiet channel conditons; measurement made at encoder output.

A.C. Characteristics — Timing Specification (1)

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

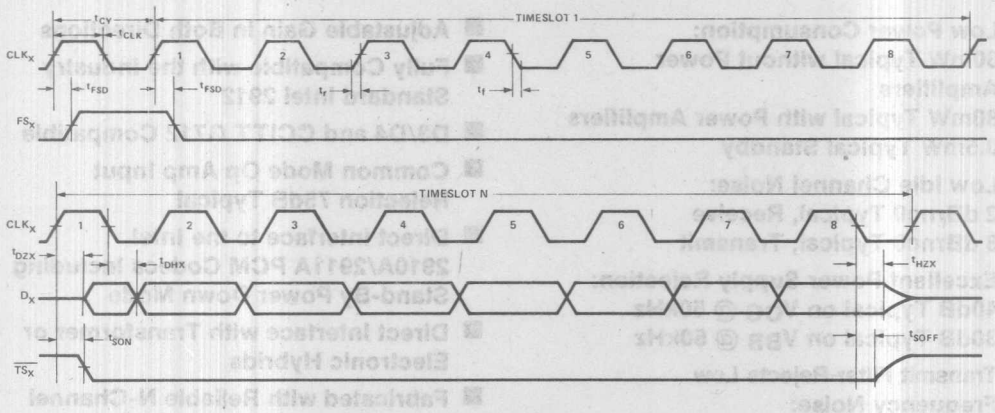
Symbol	Parameter	Limits		Units	Comments
		Min	Max		
CLOCK SECTION					
t_{CY}	Clock Period	485		ns	CLK_X, CLK_R (2.048 MHz systems), CLK_C
t_r, t_f	Clock Rise and Fall Time	0	30	ns	CLK_X, CLK_R, CLK_C
t_{CLK}	Clock Pulse Width	215		ns	CLK_X, CLK_R, CLK_C
t_{CDC}	Clock Duty Cycle ($t_{CLK} \div t_{CY}$)	45	55	%	CLK_X, CLK_R
TRANSMIT SECTION					
t_{VFX}	Analog Input Conversion	20		timeslot	from leading edge of transmit timeslot[2]
t_{DZX}	Data Enabled on TS Entry	50	180	ns	$0 < C_{LOAD} < 100$ pF
t_{DHX}	Data Hold Time	80	230	ns	$0 < C_{LOAD} < 100$ pF
t_{HZX}	Data Float on TS Exit	75	245	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	30	185	ns	$0 < C_{LOAD} < 100$ pF
t_{SOFF}	Timeslot X to Disable	70	225	ns	$C_{LOAD} = 0$
t_{FSD}	Frame Sync Delay	15	150	ns	
RECEIVE AND CONTROL SECTIONS					
t_{VFR}	Analog Output Update	9 1/16	9 1/16	timeslot	from leading edge of the channel timeslot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	60		ns	
t_{FSD}	Frame Sync Delay	15	150	ns	
t_{DSC}	Control Data Setup	115		ns	Microcomputer mode only
t_{DHC}	Control Data Hold	115		ns	Microcomputer mode only

Notes:

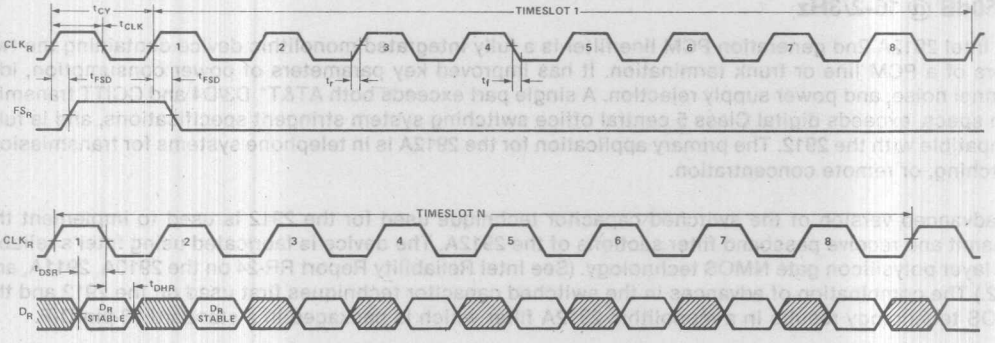
1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF}, which reference a high impedance state.
2. The 20 timeslot minimum insures that the complete A/D conversion will take place under any combination of receive interrupt or asynchronous operation of the Codec. Consult an Intel applications specialist or Intel Corporation for applications information which would allow operation with less than 20 timeslots.

TIMING WAVEFORMS [1]

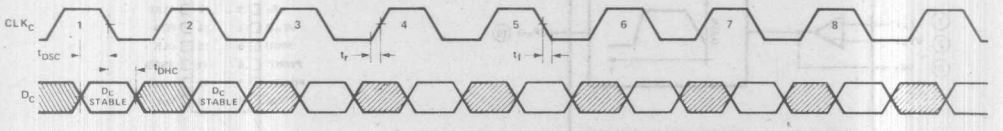
TRANSMIT TIMING



RECEIVE TIMING



CONTROL TIMING



Notes:

1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF} which reference a high impedance state.

2912A
PCM TRANSMIT/RECEIVE FILTER

- **Low Power Consumption:**
 60mW Typical without Power Amplifiers
 80mW Typical with Power Amplifiers
 0.5mW Typical Standby
- **Low Idle Channel Noise:**
 2 dBrnc0 Typical, Receive
 6 dBrnc0 Typical, Transmit
- **Excellent Power Supply Rejection:**
 40dB Typical on V_{CC} @ 50kHz
 30dB Typical on V_{BB} @ 50kHz
- **Transmit Filter Rejects Low Frequency Noise:**
 23dB @ 60Hz
 25dB @ 50Hz
 50dB @ 16-2/3Hz
- **Adjustable Gain in Both Directions**
- **Fully Compatible with the Industry Standard Intel 2912**
- **D3/D4 and CCITT G712 Compatible**
- **Common Mode Op Amp Input Rejection 75dB Typical**
- **Direct Interface to the Intel 2910A/2911A PCM Codecs Including Stand-By Power Down Mode**
- **Direct Interface with Transformer or Electronic Hybrids**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel 2912A 2nd generation PCM line filter is a fully integrated monolithic device containing the two filters of a PCM line or trunk termination. It has improved key parameters of power consumption, idle channel noise, and power supply rejection. A single part exceeds both AT&T* D3/D4 and CCITT transmission specs, exceeds digital Class 5 central office switching system stringent specifications, and is fully compatible with the 2912. The primary application for the 2912A is in telephone systems for transmission, switching, or remote concentration.

An advanced version of the switched capacitor technique used for the 2912 is used to implement the transmit and receive passband filter sections of the 2912A. The device is fabricated using Intel's reliable two layer polysilicon gate NMOS technology. (See Intel Reliability Report RR-24 on the 2910A, 2911A, and 2912.) The combination of advances in the switched capacitor techniques first used on the 2912 and the NMOS technology results in a monolithic 2912A filter which is packaged in a standard 16-pin DIP.

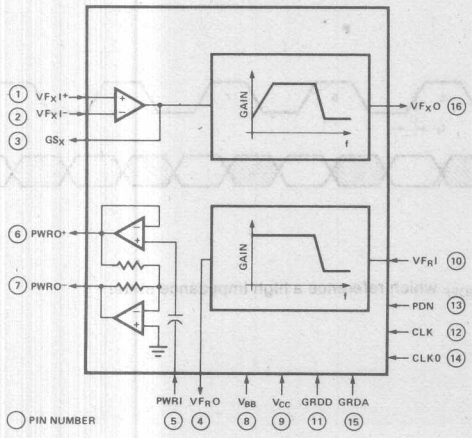
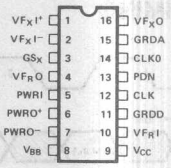


Figure 1. Block Diagram



PIN NAMES

VF_XI^+, VF_XI^-	ANALOG INPUTS	CLK	CLOCK INPUT
GS_X	GAIN CONTROL	CLK0	CLOCK SELECTION
VF_XO	ANALOG OUTPUT	PDN	POWER DOWN
VF_RI	ANALOG INPUT	V_{CC}	POWER (+5V)
VF_RO	ANALOG OUTPUT	V_{BB}	POWER (-5V)
PWRI	DRIVER INPUT	GRDD	DIGITAL GROUND
PWRO+, PWRO−	DRIVER OUTPUT	GRDA	ANALOG GROUND

Figure 2. Pin Configuration

*AT&T is a registered trademark of American Telephone and Telegraph Corporation.

Table 1. Pin Description

Symbol	Pin No.	Function	Description
VF_XI+	1	Input	Analog input of the transmit filter. The VF_XI+ signal comes from the 2 to 4 wire hybrid in the case of a 2 wire line and goes through the frequency rejection and the antialiasing filters before being sent to the Codec for encoding.
VF_XI-	2	Input	Inverting input of the gain adjustment operational amplifier on the transmit filter.
GS_X	3	Output	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
VF_RO	4	Output	Analog output of the receive filter. This output provides a direct interface to electronic hybrids. For a transformer hybrid application, VF_RO is tied to PRWI and a dual balanced output is provided on pins PWRO+ and PWRO-.
PWRI	5	Input	Input to the power driver amplifiers on the receive side for interface to transformer hybrids. High impedance input. When tied to V_{BB}, the power amplifiers are powered down.
PWRO+	6	Output	Non-inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
PWRO-	7	Output	Inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
V_{BB}	8	Power	-5V ±5% referenced to GRDA
V_{CC}	9	Power	+5V ±5% referenced to GRDA

Symbol	Pin No.	Function	Description
VF_RI	10	Input	Analog input of the receive filter, interface to the Codec analog output for PCM applications. The receive filter provides the $\frac{Sinx}{x}$ correction needed for sample and hold type Codec outputs to give unity gain. The input voltage range is directly compatible with the Intel 2910A and 2911A Codecs.
GRDD	11	Ground	Digital ground return for internal clock generator.
CLK[1]	12	Input	Clock input. Three clock frequencies can be used: 1.536MHz, 1.544MHz or 2.048MHz; pin 14, CLK0, has to be strapped accordingly. High impedance input, TTL voltage levels.
PDN	13	Input	Control input for the stand-by power down mode. An internal pull up to +5V is provided for interface to the Intel 2910A and 2911A PDN outputs. TTL voltage levels.
CLK0[1]	14	Input	Clock (pin 12, CLK) frequency selection. If tied to V_{BB}, CLK should be 1.536MHz. If tied to Ground, CLK should be 1.544 MHz. If tied to V_{CC}, CLK should be 2.048MHz.
GRDA	15	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
VF_XO	16	Output	Analog output of the transmit filter. The output voltage range is directly compatible with the Intel 2910A and 2911A Codecs.

NOTE:

1. The three clock frequencies are directly compatible with the Intel 2910A and 2911A Codecs. The following table should be observed in selecting the clock frequency.

Codec Clock	Clock Bits/Frame	CLK, Pin 12	CLK0, Pin 14
1.536 MHz	192	1.536 MHz	V_{BB} (-5V)
1.544 MHz	193	1.544 MHz	GRDD
2.048 MHz	256	2.048 MHz	V_{CC} (+5V)

FUNCTIONAL DESCRIPTION

The 2912A provides the transmit and receive filters found on the analog termination of a PCM line or trunk. The transmit filter performs the anti-aliasing function needed for an 8KHz sampling system, and the 50/60Hz rejection. The receive filter has a low pass transfer characteristic and also provides the Sinx/x correction necessary to interface the Intel 2910A (μ Law) and 2911A (A Law) Codecs which have a non-return-to-zero output of the digital to analog conversion. Gain adjustment is provided in the receive and transmit directions.

A stand-by, power down mode is included in the 2912A and can be directly controlled by the 2910A/2911A Codecs.

The 2912A can interface directly with a transformer hybrid (2 to 4 wire conversion) or with electronic hybrids; in the latter case the power dissipation is reduced by powering down the output amplifier provided on the 2912A.

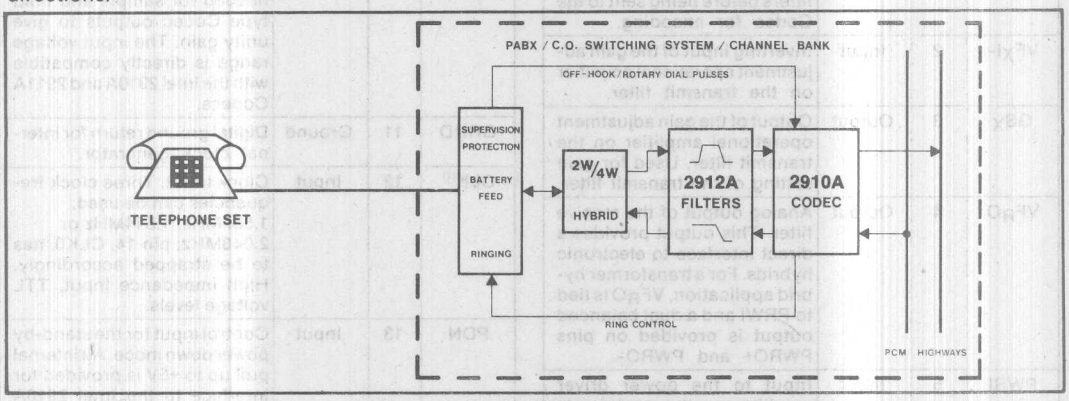


Figure 3. Typical Line Termination

FILTER OPERATION

Transmit Filter Input Stage

The input stage provides gain adjustment in the pass-band. The input operational amplifier has a common mode range of ±2.2 volts, a DC offset of less than 25mV, a voltage gain greater than 3000 and a unity gain bandwidth of 1 MHz. It can be connected to provide a gain of 20dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output (GS_X) must be greater than 10KΩ in parallel with 25 pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of +3dB in the pass band.

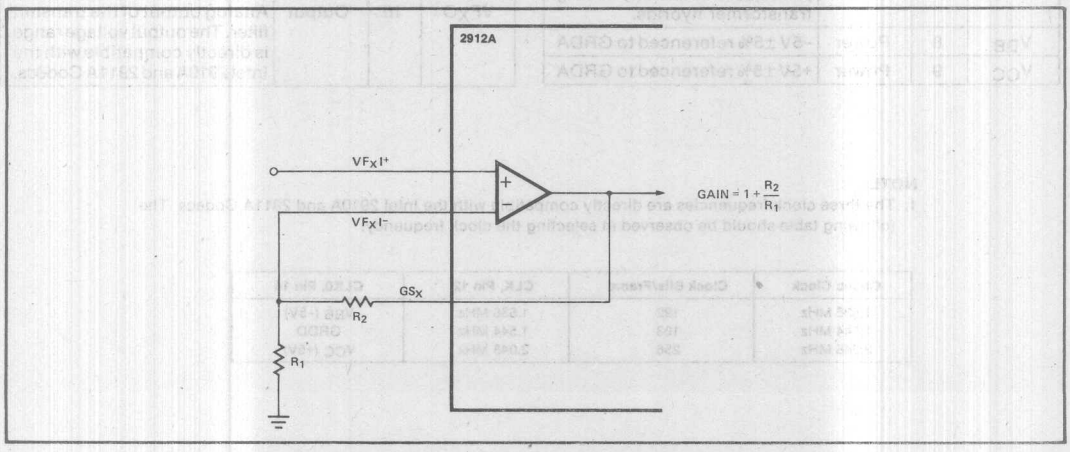


Figure 4. Transmit Filter Gain Adjustment

Receive Filter Output

The VF_RO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VF_RI to VF_RO is:

$$\frac{\left(\frac{\pi f}{8000}\right)}{\text{Sin}\left(\frac{\pi f}{8000}\right)}$$

which when multiplied by the output response of the Intel 2910A and 2911A Codecs results in a 0dB gain in the pass band. The filter gain can be adjusted downward by a resistor voltage divider connected as shown. The total resistive load R_{LR} on VF_RO should not be less than 10k Ω.

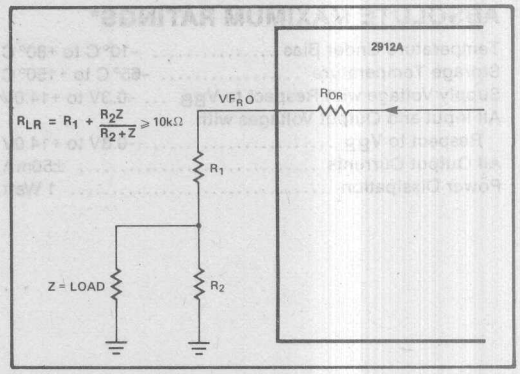


Figure 5. Receive Filter Output Gain Adjustment

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VF_RO is connected through gain setting resistors R_1 and R_2 to the amplifier input PWRI. The input voltage range on PWRI is ±3.2 volts and the gain is 6dB for a bridged output. With a 600Ω load connected between PWRO+ and PWRO−, the maximum voltage swing across the load is ±5.0 volts. The series combination of R_S and the hybrid transformer must present a minimum A.C. load resistance of 600Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown below. These amplifiers can also be used with loads connected to ground.

When the power amplifier is not needed it should be deactivated to save power. This is accomplished by tying the PWRI pin to V_{BB} before the device is powered up.

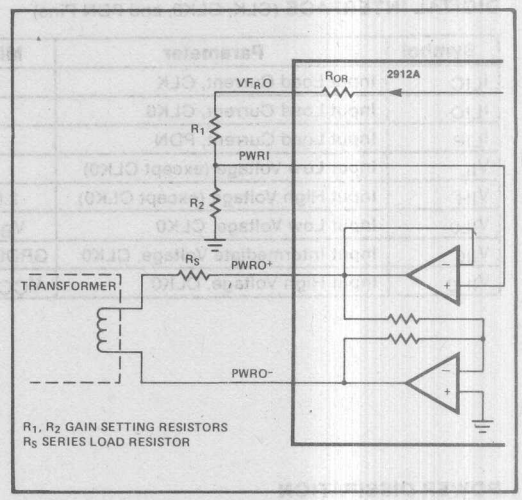


Figure 6. Typical Connection of Output Driver Amplifier

Power Down Mode

Pin 13, PDN, provides the power down control. When the signal on this lead is brought high, the 2912A goes into a standby, power down mode. Power dissipation is reduced to 0.5mW. In the stand-by mode, all outputs go into a high impedance state. This feature allows multiple 2912As to drive the same analog bus on a time-shared basis.

When power is restored, the settling time of the 2912A is typically 15ms.

The PDN interface is directly compatible with the Intel 2910A and 2911A PDN outputs. Only one command from the common control is then necessary to power down both the Codec and the Filters of the line or trunk interface.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias -10° C to +80° C
Storage Temperature -65° C to +150° C
Supply Voltage with Respect to V_{BB} ... -0.3V to +14.0V
All Input and Output Voltages with
Respect to V_{BB} -0.3V to +14.0V
All Output Currents ±50mA
Power Dissipation 1 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0° C to +70° C; V_{CC} =5V ±5%; V_{BB} = -5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified.)

DIGITAL INTERFACE (CLK, CLK0, and PDN Pins)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{LIC}	Input Load Current, CLK			10	μA	V_{IN} = GRDD to V_{CC}
I_{LIO}	Input Load Current, CLK0			10	μA	V_{IN} = V_{BB} to V_{CC}
I_{LIP}	Input Load Current, PDN			-100	μA	V_{IN} = GRDD to V_{CC}
V_{IL}	Input Low Voltage (except CLK0)			0.8	V	
V_{IH}	Input High Voltage (except CLK0)	2.0			V	
V_{IL0}	Input Low Voltage, CLK0	V_{BB}		$V_{BB}^{+0.5}$	V	
V_{II0}	Input Intermediate Voltage, CLK0	$GRDD^{-0.5}$		0.8	V	
V_{IH0}	Input High Voltage, CLK0	$V_{CC}^{-0.5}$		V_{CC}	V	

POWER DISSIPATION

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{CC0}	V_{CC} Standby Current		50	100	μA	PDN = V_{IH} MIN
I_{BB0}	V_{BB} Standby Current		50	100	μA	PDN = V_{IH} MIN
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive		6	10	mA	PWRI = V_{BB}[2]
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive		6	10	mA	PWRI = V_{BB}[2]
I_{CC2}	V_{CC} Operating Current		8	14	mA	
I_{BB2}	V_{BB} Operating Current		8	14	mA	

NOTE:
1. Typical values are for T_A = 25°C and nominal power supply values.
2. To place the power amplifiers in the inactive mode PWRI must be tied to V_{BB} prior to power-up.

D.C. CHARACTERISTICS

(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{BB} = -5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified.)

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{BXI}	Input Leakage Current, VF_XI+, VF_XI-			100	nA	$-2.2V < V_{IN} < 2.2V$
R_{IXI}	Input Resistance, VF_XI+, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-			25	mV	
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	60	75		dB	$-2.2V < V_{IN} < -2.2V$, 0dBmO≡ $1.1V_{RMS}$, Input at VF_XI-
A_{VOL}	DC Open Loop Voltage Gain, GS_X	3000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		1		MHz	
V_{OXI}	Output Voltage Swing, GS_X	±2.5			V	$R_L \geq 10k\Omega$
C_{LXI}	Load Capacitance, GS_X			25	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	Minimum R_L

ANALOG INTERFACE, TRANSMIT FILTER (See Figure 9)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
R_{OX}	Output Resistance, VF_XO		20	35	Ω	
V_{OSX}	Output DC Offset, VF_XO			100	mV	VF_XI+ Connected to GRDA, Input Op Amp at Unity Gain
$PSRR_1$	Power Supply Rejection of V_{CC} at 1kHz, VF_XO	30	40		dB	Note 2
$PSRR_2$	Power Supply Rejection of V_{BB} at 1kHz, VF_XO	25	30		dB	Note 2
C_{LX}	Load Capacitance, VF_XO			25	pF	
R_{LX}	Minimum Load Resistance, VF_XO	2.7			kΩ	Minimum R_L
V_{OX1}	Output Voltage Swing, 1kHz, VF_XO	±3.2			V	$R_L \geq 10k\Omega$ or with 2910A or 2911A
V_{OX2}	Output Voltage Swing, 1kHz, VF_XO	±2.5			V	$R_L \geq 2.7\ k\Omega$

ANALOG INTERFACE, RECEIVE FILTER (See Figure 10)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{BR}	Input Leakage Current, VF_RI			3	μA	$-3.2V < V_{IN} < 3.2V$
R_{IR}	Input Resistance, VF_RI	1			MΩ	
R_{OR}	Output Resistance, VF_RO			100	Ω	
V_{OSR}	Output DC Offset, VF_RO			100	mV	VF_RI Connected to GRDA
$PSRR_3$	Power Supply Rejection of V_{CC} at 1kHz, VF_RO	30	45		dB	
$PSRR_4$	Power Supply Rejection of V_{BB} at 1kHz, VF_RO	30	35		dB	
C_{LR}	Load Capacitance, VF_RO			25	pF	
R_{LR}	Minimum Load Resistance, VF_RO	10			kΩ	Minimum R_L
V_{OR}	Output Voltage Swing, VF_RO	±3.2			V	R_L = 10kΩ

NOTE:

1. Typical values for T_A = 25°C and nominal power supply values.
2. $PSRR_{1,2}$ include input op amp in transmit section.

D.C. CHARACTERISTICS

(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{BB} = -5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified.)

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{BRA}	Input Leakage Current, PWRI			3	μA	-3.2V < V_{IN} < 3.2V
R_{IRA}	Input Resistance, PWRI	10			MΩ	
R_{ORA}	Output Resistance, PWRO+, PWRO-		1		Ω	$\lvert I_{OUT}\rvert$ < 10mA -3.0V < V_{OUT} < 3.0V
V_{OSRA}	Output DC Offset, PWRO+, PWRO-			50	mV	PWRI Connected to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO-			100	pF	
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO- Single Ended Connection	±3.2			V	R_L = 10kΩ; R_L Connected to GRDA for ⩾ 200 Hz
		±2.9			V	R_L = 600Ω
		±2.5			V	R_L = 300Ω
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO- Balanced Output Connection	±6.4			V	R_L = 20kΩ; R_L Connected Between PWRO+ and PWRO- for ⩾ 200 Hz
		±5.8			V	R_L = 1200Ω
		±5.0			V	R_L = 600Ω

A.C. CHARACTERISTICS

(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{BB} = -5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified.)

Clock Input Frequency: CLK = 1.536MHz ±0.1%; CLK0 = V_{IL0} (Tied to V_{BB}) CLK = 2.048MHz ±0.1%; CLK0 = V_{IH0} (Tied to V_{CC})
CLK = 1.544MHz ±0.1%; CLK0 = V_{IL0} (Tied to GRDD)

TRANSMIT FILTER TRANSFER CHARACTERISTICS (See Transmit Filter Transfer Characteristics, Figure 7)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1kHz					0dBmO Input Signal
	16.67Hz		-56	-50	dB	Gain Setting Op Amp at Unity Gain
	50Hz			-25	dB	
	60Hz			-23	dB	
	200Hz	-1.0		-0.125	dB	0dBmO Signal ≡ 1.1 V_{RMS} Input at VF_XI-
	300Hz to 3000Hz	-0.125		0.125	dB	
	3300Hz	-.35		0.03	dB	
	3400Hz	-0.7		-0.1	dB	0dBmO Signal ≡ 1.6 V_{RMS} Output at VF_XO
	4000Hz			-14	dB	
	4600Hz and Above			-32	dB	
G_{AX}	Absolute Passband Gain at 1kHz, VF_XO	2.9	3.0	3.1	dB	R_L = ∞, Note 3
G_{AXT}	Gain Variation with Temperature at 1kHz		.0002	.002	dB/°C	0dBmO Signal Level
G_{AXS}	Gain Variation with Supplies at 1kHz		.01	.07	dB/V	0dBmO Signal Level, Supplies ±5%
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO $20 \log \frac{VF_XO}{VF_RO}$		-75	-65	dB	VF_RI = 1.6 V_{RMS}, 1kHz Input VF_XI+, VF_XI- Connected to GS_X, GS_X Connected through 10kΩ to GRDA
N_{CX1}	Total C Message Noise at Output, VF_XO		6	11	dBrnc0 \|2\|	Gain Setting Op Amp at Unity Gain
N_{CX2}	Total C Message Noise at Output, VF_XO		9	13	dBrnc0 \|2\|	Gain Setting Op Amp at 20dB Gain
D_{DX}	Differential Envelope Delay, VF_XO 1kHz to 2.6kHz			60	μs	
D_{AX}	Absolute Delay at 1kHz, VF_XO			110	μs	
DP_{X1}	Single Frequency Distortion Products			-48	dB	0dBm0 Input Signal at 1kHz
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3dBm0 at VF_XO			-45	dB	0.16 V_{RMS} 1kHz Input Signal at VF_XI+; Gain Setting Op Amp at 20dB Gain. The +3dBmO signal at VF_XO is 2.26 V_{RMS}

See next page for **NOTES.**

A.C. CHARACTERISTICS

(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{BB} = -5V ±5%; GRDA = 0V; GRDD = 0V; unless otherwise specified.)
Clock Input Frequency: CLK = 1.536MHz ±0.1%; CLK0 = V_{IL0} (Tied to V_{BB})
CLK = 1.544MHz ±0.1%; CLK0 = V_{II0} (Tied to GRDD)
CLK = 2.048MHz ±0.1%; CLK0 = V_{IH0} (Tied to V_{CC})

RECEIVE FILTER TRANSFER CHARACTERISTICS (See Receive Filter Transfer Characteristics, Figure 8)

Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1kHz with Sinx/x Correction of 2910A or 2911A					0dBmO Input Signal
	Below 200Hz			0.125	dB	0dBmO Signal ≡ 1.6 V_{RMS} x $\text{Sin}\left(\frac{\pi f}{8000}\right)\Big/\left(\frac{\pi f}{8000}\right)$
	200Hz	-0.5		0.125	dB	
	300Hz to 3000Hz	-0.125		0.125	dB	
	3300Hz	-.35		0.03	dB	Input at VF_RI
	3400Hz	-0.7		-0.1	dB	
	4000Hz			-14	dB	
	4600Hz and Above			-30	dB	
G_{AR}	Absolute Passband Gain at 1kHz, VF_RO	-0.1	0	+0.1	dB	R_L = ∞, Notes 3, 4
G_{ART}	Gain Variation with Temperature at 1kHz		.0002	.002	dB/°C	0dBmO Signal Level
G_{ARS}	Gain Variation with Supplies at 1kHz		.01	.07	dB/V	0dBmO Signal Level, Supplies ±5%
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO; 20 log (VF_RO/VF_XO)		-70	-60	dB	VF_XI = 1.1 V_{RMS}, 1kHz Output VF_RI Connected to GRDA
N_{CR}	Total C Message Noise at Output, VF_RO		2	6	dBrnc0 [2]	VF_RO Output or PWRO+ and PWRO- Connected with Unity Gain
D_{DR}	Differential Envelope Delay, VF_RO, 1kHz to 2.6kHz			100	μs	
D_{AR}	Absolute Delay at 1kHz, VF_RO			110	μs	
DP_{R1}	Single Frequency Distortion Products			-48	dB	0dBm0 Input Signal at 1kHz
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3dBm0 at VF_RO			-45	dB	+3dBmO Signal Level of 2.26 V_{RMS}, 1kHz Input at VF_RI

NOTES:
1. Typical values are for T_A = 25°C and nominal power supply values.
2. A noise measurement of 12dBrnc into a 600Ω load at the 2912A device is equivalent to 6dBrnc0.
3. For gain under load refer to output resistance specs and perform gain calculation.
4. Output is non-inverting.

TRANSFER CHARACTERISTICS

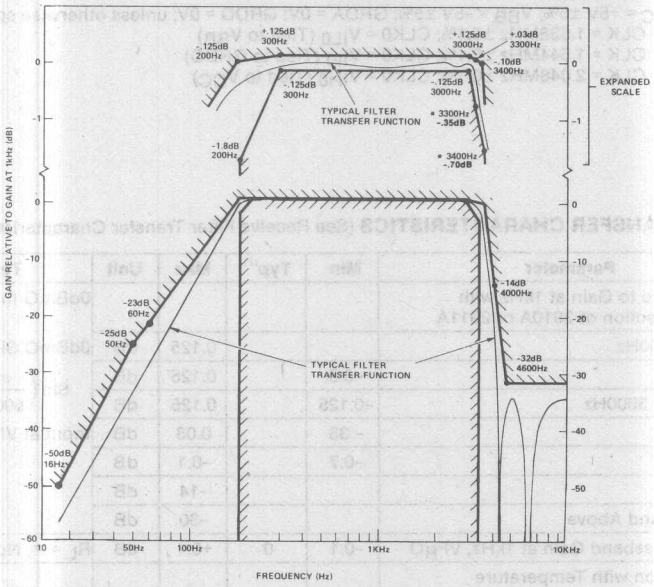
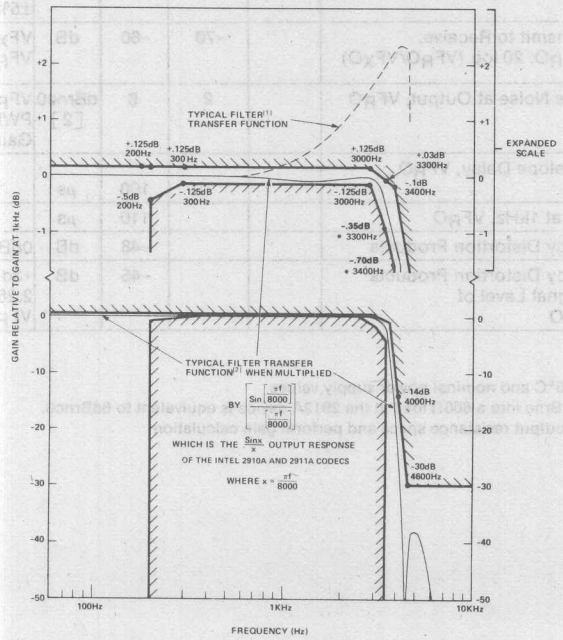


Figure 7. Transmit Filter



NOTES:
1. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER AS A SEPARATE COMPONENT.
2. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER DRIVEN BY THE SAMPLE AND HOLD OUTPUT OF THE INTEL 2910A AND 2911A CODECS. THE COMBINED FILTER/CODEC RESPONSE MEETS THE STATED SPECIFICATIONS.

Figure 8. Receive Filter

POWER SUPPLY REJECTION TYPICAL VALUES OVER 3 RANGES

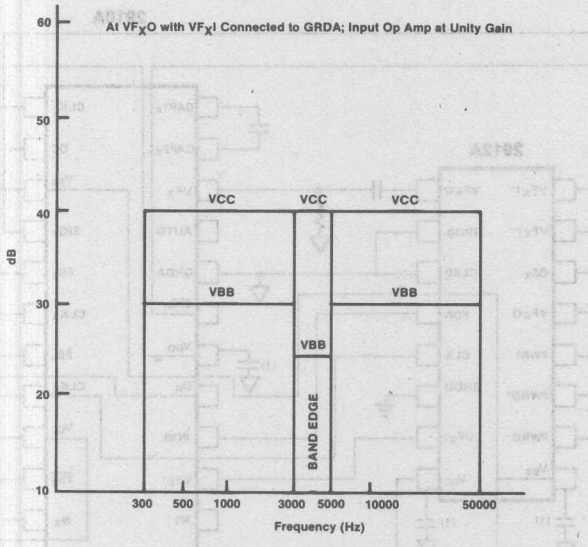


Figure 9. Transmit Filter

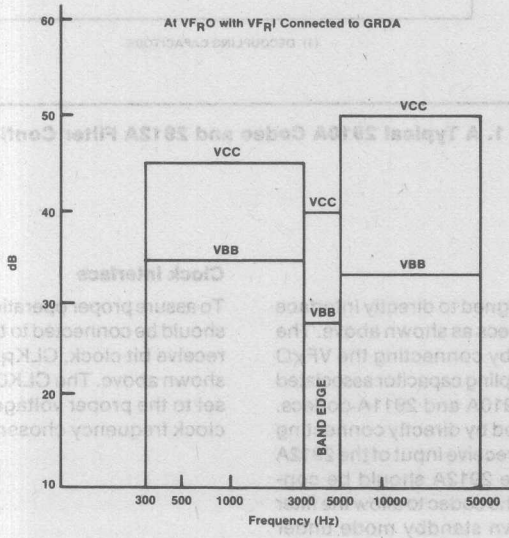


Figure 10. Receive Filter

APPLICATIONS INFORMATION
2910A/2911A/2912A

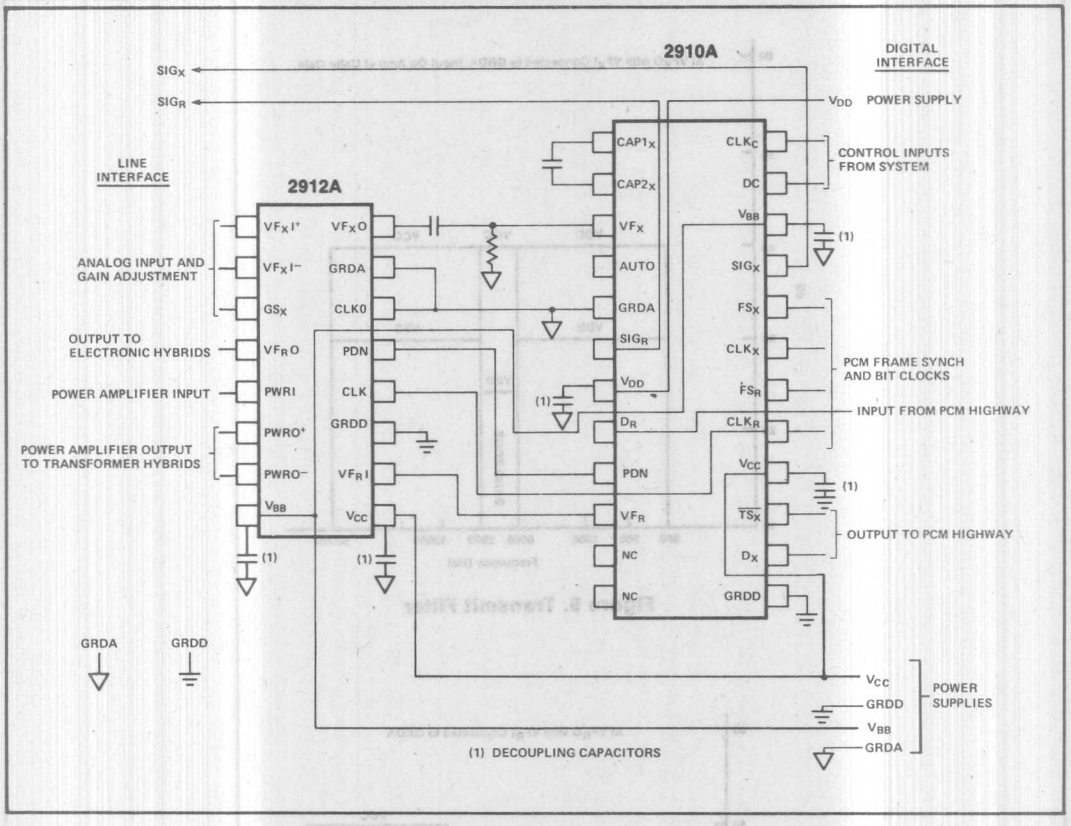


Figure 1. A Typical 2910A Codec and 2912A Filter Configuration

Codec Interface

The 2912A PCM Filter is designed to directly interface to the 2910A and 2911A Codecs as shown above. The transmit path is completed by connecting the VF_XO output of the 2912A to the coupling capacitor associated with the VF_X input of the 2910A and 2911A codecs. The receive path is completed by directly connecting the codec output VF_R to the receive input of the 2912A VF_RI. The PDN input of the 2912A should be connected to the PDN output of the codec to allow the filter to be put in the power-down standby mode under control of the codec.

Clock Interface

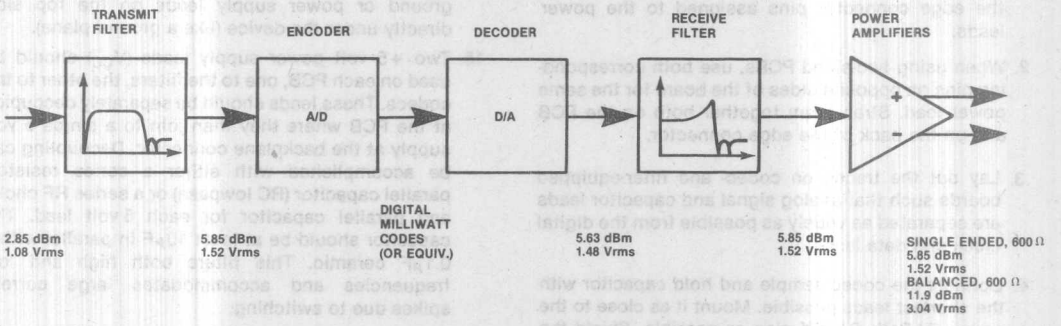
To assure proper operation, the CLK input of the 2912A should be connected to the same clock provided to the receive bit clock, CLK_R of 2910A or 2911A Codec as shown above. The CLK0 input of the 2912A should be set to the proper voltage depending on the standard clock frequency chosen for the codec and filter.

Grounding, Decoupling, and Layout Recommendations

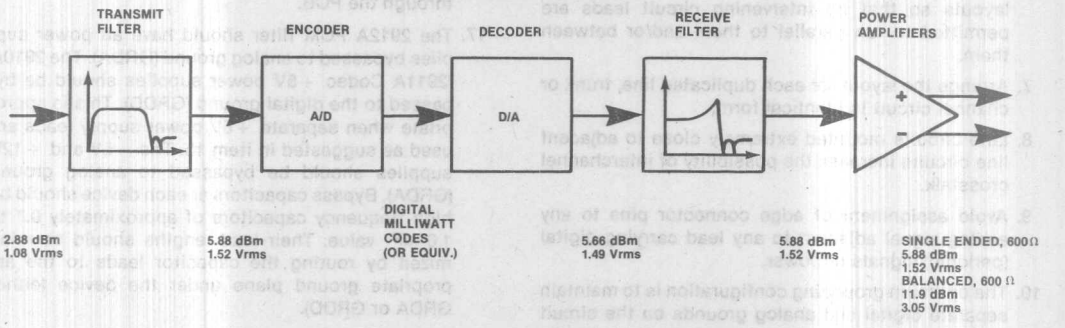
The most important steps in designing a low noise line card are to insure that the layout of the circuit components and traces results in a minimum of cross coupling between analog and digital signals, and to provide well bypassed and clean power supplies, solid ground planes, and minimal lead lengths between components.

1. All power source leads should be bypassed to ground on each printed circuit board (PCB), on which codecs are provided. At least one electrolytic bypass capacitor (at least 50 μF) per board is recommended at the point where all power traces from the codecs and filters join prior to interfacing with the edge connector pins assigned to the power leads.
2. When using two-sided PCBs, use both corresponding pins on opposite sides of the board for the same power lead. Strap them together both on the PCB and on the back of the edge connector.
3. Lay out the traces on codec- and filter-equipped boards such that analog signal and capacitor leads are separated as widely as possible from the digital clock and data leads.
4. Connect the codec sample and hold capacitor with the shortest leads possible. Mount it as close to the codec CAP1X, CAP2X pins as possible. Shield the capacitor traces with analog ground.
5. Do not lay out any board traces (especially digital) that pass between or near the leads of the sample and hold capacitor(s) since they are in high impedance circuits which are sensitive to noise coupling.
6. Keep analog voice circuit leads paired on their layouts so that no intervening circuit leads are permitted to run parallel to them and/or between them.
7. Arrange the layout for each duplicated line, trunk or channel circuit in identical form.
8. Line circuits mounted extremely close to adjacent line circuits increase the possibility of interchannel crosstalk.
9. Avoid assignment of edge connector pins to any analog signal adjacent to any lead carrying digital (periodic) signals or power.
10. The optimum grounding configuration is to maintain separate digital and analog grounds on the circuit boards, and to carry these grounds back to the power supply with a low impedance connection. This keeps the grounds separate over the entire system except at the power supply.
11. The voltage difference between ground leads GRDA and GRDD (analog and digital ground) should not exceed two volts. One method of preventing any substantial voltage difference between leads GRDA and GRDD is to connect two diodes back to back in opposite directions across these two ground leads on each board.
12. Codec-filter pairs should be aligned so that pins 9 through 16 of the filter face pins 1 through 12 of the codec. This minimizes the distance for analog connections between devices and with no crossing analog lines.
13. No digital or high voltage level (such as ringing supply) lines should run under or in parallel with these analog VF connections. If the analog lines are on the top (component side) of the PC board, then GRDD, GRDA, or power supply leads should be directly under them, on the bottom to prevent analog/digital coupling.
14. Both the codec and filter devices should be shielded from traces on the bottom of the PCB by using ground or power supply leads on the top side directly under the device (like a ground plane).
15. Two +5 volt power supply leads (V_{CC}) should be used on each PCB, one to the filters, the other to the codecs. These leads should be separately decoupled at the PCB where they then join to a single 5 volt supply at the backplane connector. Decoupling can be accomplished with either a series resistor/parallel capacitor (RC lowpass) or a series RF choke and parallel capacitor for each 5 volt lead. The capacitor should be at least 10μF in parallel with a 0.1μF ceramic. This filters both high and low frequencies and accommodates large current spikes due to switching.
16. Both grounds and power supply leads must have low resistance and inductance. This should be accomplished by using a ground plane whenever possible. When narrower traces must be used, a minimum width of 4 millimeters should be maintained. Either multiple or extra large plated through holes should be used when passing the ground connections through the PCB.
17. The 2912A PCM filter should have all power supplies bypassed to analog ground (GRDA). The 2910A /2911A Codec +5V power supplies should be bypassed to the digital ground (GRDD). This is appropriate when separate +5V power supply leads are used as suggested in item 15. The −5V and +12V supplies should be bypassed to analog ground (GRDA). Bypass capacitors at each device should be high frequency capacitors of approximately 0.1 to 1.0 μF value. Their lead lengths should be minimized by routing the capacitor leads to the appropriate ground plane under the device (either GRDA or GRDD).
18. Relay operation, ring voltage application, interruptions, and loop current surges can produce enormous transients. Leads carrying such signals must be routed well away from both analog and digital circuits on the line card and in backplanes. Lead pairs carrying current surges should be routed closely together to minimize possible inductive coupling. The microcomputer clock lead is particularly vulnerable, and should be buffered. Care should also be used in the backplane layout to prevent pick-up surges. Any other latching components (relay buffers, etc.) should also be protected from surges.

2910A/2912A 0dBm0



2911A/2912A 0dBm0



Combined Single Chip PCM Codec and Filter

2

Combined Single Chip PCM Codec and Filter

2

PRELIMINARY

2913 AND 2914
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- **2914 Asynchronous clocks, 8th bit signaling, loop back test capability**
- **2913 Synchronous clocks only, 300 mil package**

- **AT&T D3/D4 and CCITT Compatible**
- **Pin Selectable μ-law or A-law Operation**
- **Two Timing Modes:**
 - **—Fixed Data Rate Mode 1.536, 1.544, or 2.048 MHz**
 - **—Variable Data Rate Mode 64 kHz-4.096 MHz**
- **Exceptional Analog Performance**
- **Low Power HMOS-E Technology:**
 - **—5mW Typical Power Down**
 - **—140mW Typical Operating**
- **Fully Differential Architecture Enhances Noise Immunity**
- **On-Chip Auto Zero, Sample and Hold, and Precision Voltage References**
- **Direct Interface with Transformer or Electronic Hybrids**

The Intel 2913 and 2914 are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven N-channel HMOS silicon gate technology. These devices provide the functions that were formerly provided by two complex chips (2910A or 2911A and 2912A). Besides the higher level of integration, the performance of the 2913 and 2914 is superior to that of the separate devices.

The primary applications for the 2913 and 2914 are in telephone systems:

- Switching—Digital PBX's and Central Office Switching Systems
- Transmission—D3/D4 Type Channel Banks and Subscriber Carrier Systems
- Subscriber Instruments—Digital Handsets and Office Workstations

The wide dynamic range of the 2913 and 2914 (78 dB) and the minimal conversion time make them ideal products for other applications such as:

- Voice Store and Forward
- Digital Echo Cancellers
- Secure Communications Systems
- Satellite Earth Stations

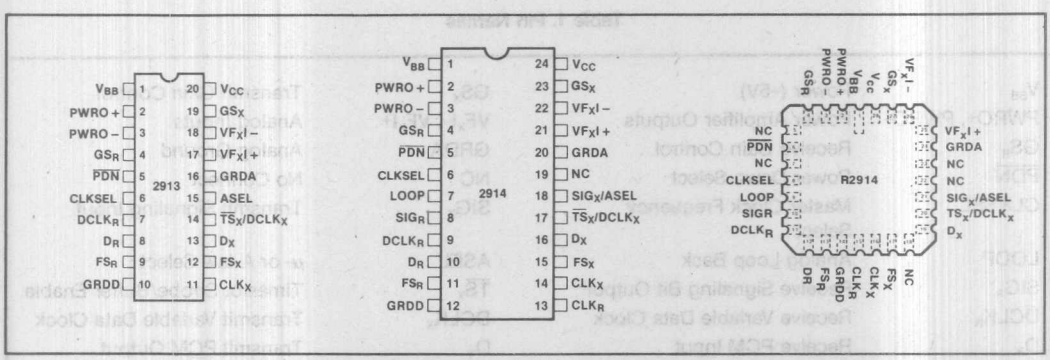


Figure 1. Pin Configurations

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September 1983
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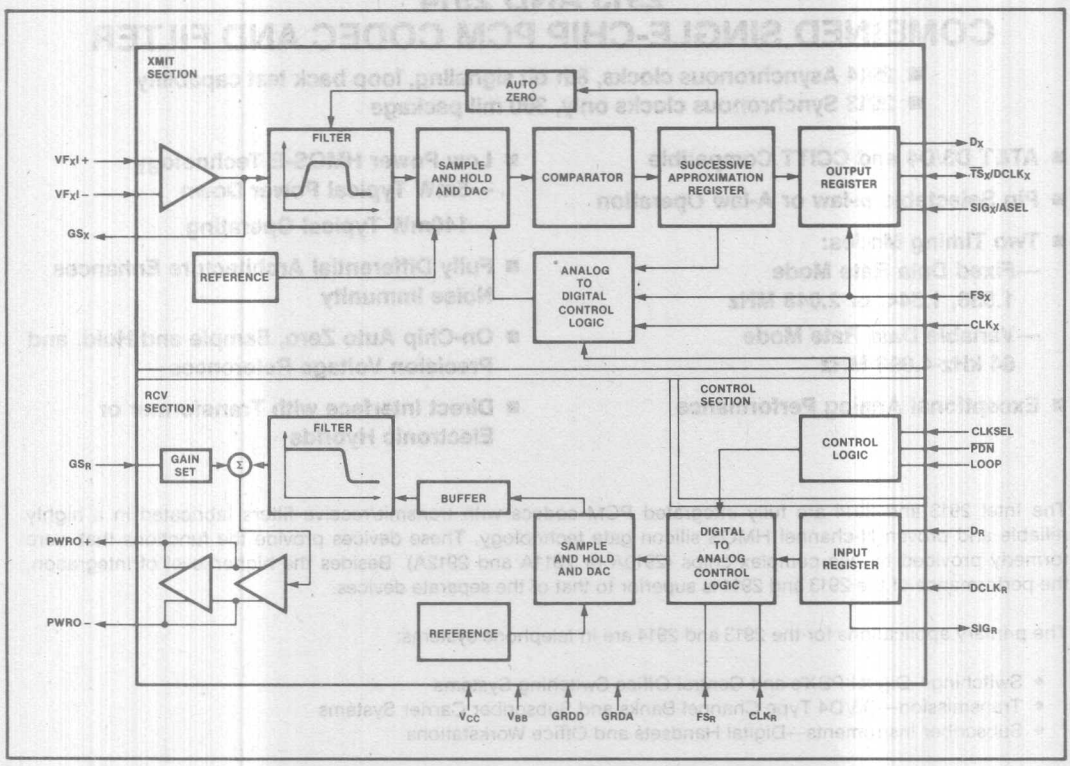


Figure 2. Block Diagram

Table 1. Pin Names

V_{BB}	Power (–5V)	GS_X	Transmit Gain Control
PWRO+, PWRO–	Power Amplifier Outputs	$VF_XI–$, VF_XI+	Analog Inputs
$\overline{GS_R}$	Receive Gain Control	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG_X	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-law Select
SIG_R	Receive Signaling Bit Output	$\overline{TS_X}$	Timeslot Strobe/Buffer Enable
$DCLK_R$	Receive Variable Data Clock	$DCLK_X$	Transmit Variable Data Clock
D_R	Receive PCM Input	D_X	Transmit PCM Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

Table 2. Pin Description

Symbol	Function
V_{BB}	Most negative supply; input voltage is –5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO–	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} 2.048 MHz CLKSEL = GRDD 1.544 MHz CLKSEL = V_{CC} 1.536 MHz
LOOP	Analog loopback. When this pin is TTL high, the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO–, and VF_XI- is internally connected to GS_X. A 0dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
SIG_R	Signaling bit output, receive channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/ timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 300 milliseconds.
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/ timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 300 milliseconds.
D_X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
SIG_X/ASEL	A dual purpose pin. When connected to V_{BB}, A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	No connect
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 2913 and 2914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

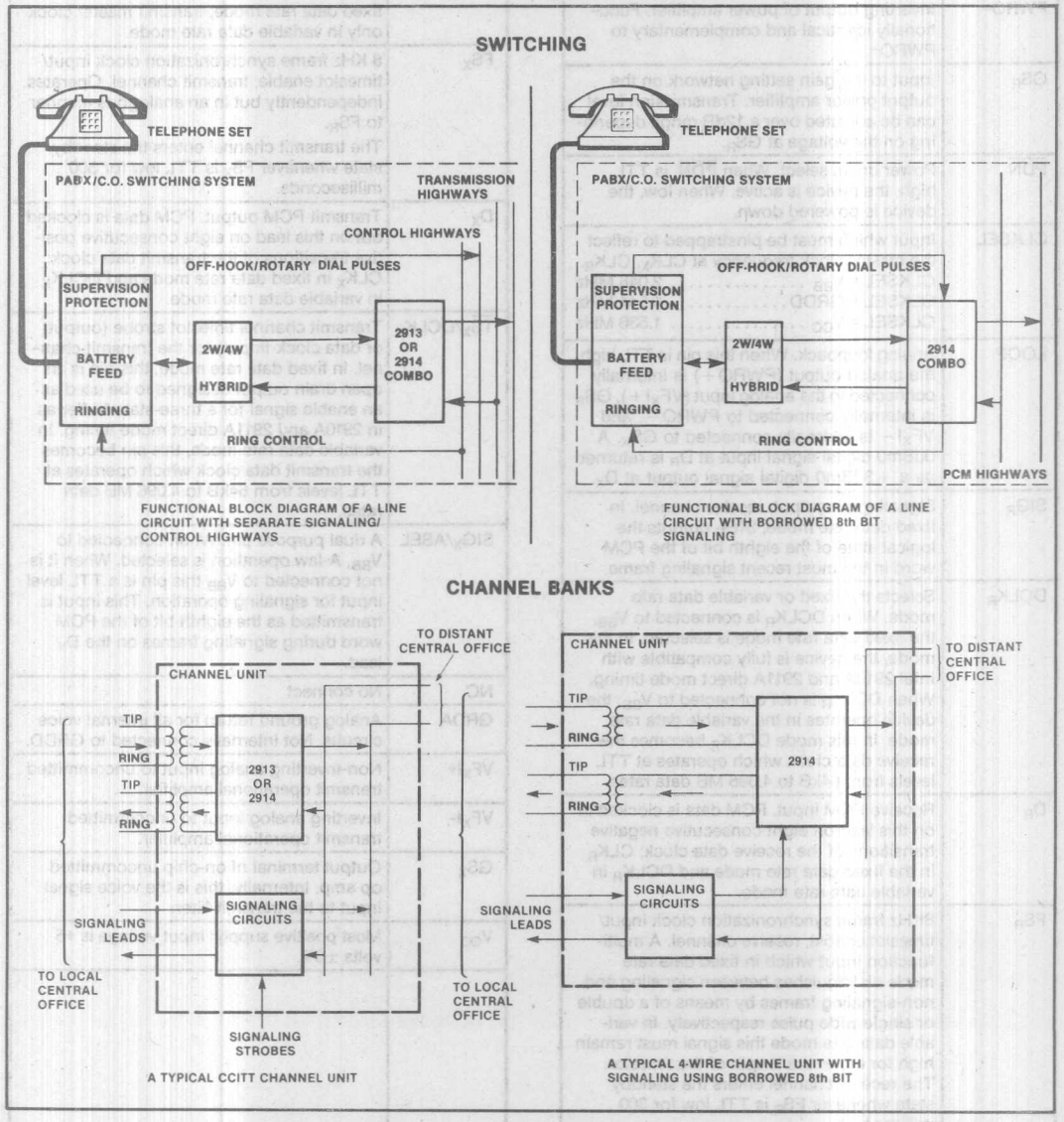


Figure 3. Typical Line Terminations

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The 2913 and 2914 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500μs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X, $\overline{TS}_X$, and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit settling time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 20μs after an interruption of CLK_X. Similarly, SIG_R will be held low approximately 20μs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 2913/2914 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 5 milliwatts. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 12 milliwatts. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clocks CLK_X and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. $\overline{TS}_X$ is a timeslot strobe/buffer

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	5 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 μs
Standby Mode	FS_X and FS_R are TTL low	12 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 300 milliseconds after FS_X and FS_R are removed.
Only transmit is on standby	FS_X is TTL low	70 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	110 mW	SIG_R is placed in a TTL low state within 300 milliseconds.

enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544, or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the 2914 or synchronous in the case of the 2913, from 64 kHz to 4.096 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125μs frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Signaling

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R = V_{BB}$). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in Figure 4.

Asynchronous Operation

The 2914 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special inter-

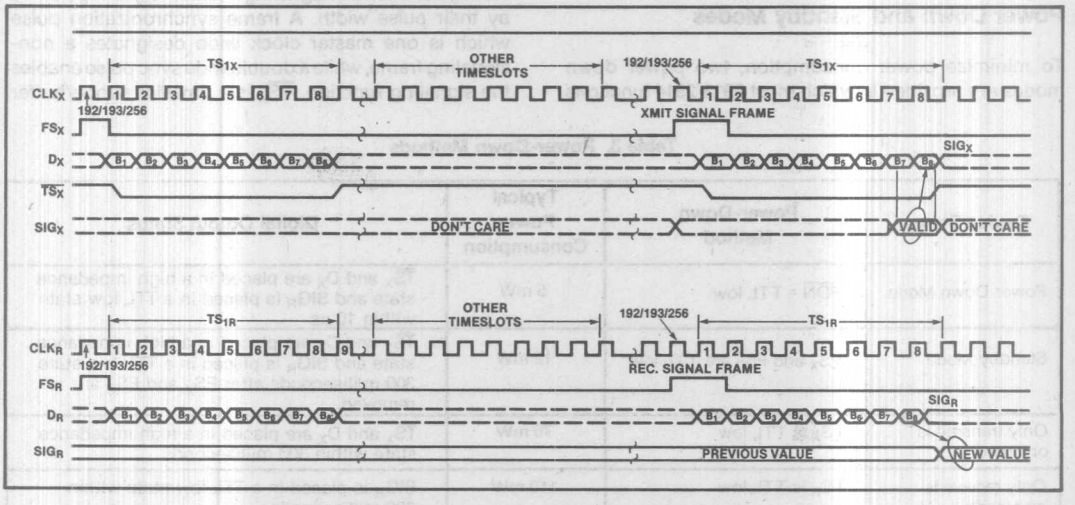


Figure 4. Signaling Timing (Used Only with Fixed Data Rate Mode)

rupt circuitry, the design of the Intel 2913/2914 combochip includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in variable data rate mode the rising edge of CLK_X must occur within t_{FSD} nanoseconds before the rise of FS_X, while the leading edge of $DCLK_X$ must occur within t_{TSDX} nanoseconds of the rise of FS_X. Thus, CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagrams, page 18). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

Analog Loopback

A distinctive feature of the 2914 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in Figure 5, when LOOP is TTL high the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO−, and VF_XI- is internally connected to GS_X.

With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a 0 dBm0 code sent into D_R will emerge from D_X as a +3dBm0 code, an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses a difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

Conversion Laws

The 2913 and 2914 are designed to operate in both μ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for μ-law and A-law conversion. If

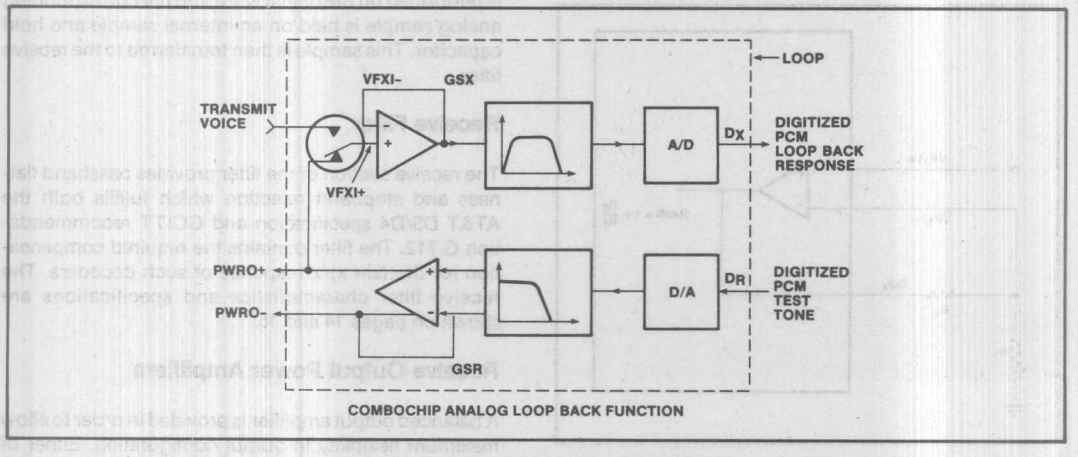


Figure 5. Simplified Block Diagram of 2914 Combochip in the Analog Loopback Configuration

A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If μ = 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB of the PCM output in signaling frames.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see Figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The 2913 and 2914 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown on pages 14 and 15.

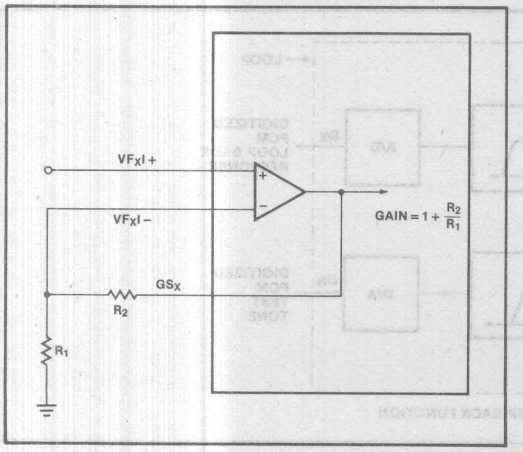


Figure 6. Transmit Filter Gain Adjustment

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications are shown on pages 14 and 15.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to

GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12 dBM or 600 ohms differentially to a level of 15 dBM.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO–, the receive level is maximized; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and –12 dB as GS_R is interpolated (with a potentiometer) between PWRO+ and PWRO–. The use of the output gain set is illustrated in Figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET: DESIGN CONSIDERATIONS

(Refer to Figure 7.)

PWRO+ and PWRO– are low impedance complementary outputs. The voltages at the nodes are:

Vo+ at PWRO+

Vo– at PWRO–

Vo = Vo+ – Vo– (total differential response)

R_1 and R_2 are a gain setting resistor network with the center tap connected to the GS_R input.

A value greater than 10K ohms and less than 100K for $R_1 + R_2$ is recommended because:

(a) The parallel combination of $R_1 + R_2$ and R_L sets the total loading.

(b) The total capacitance at the GS_R input and the parallel combination of R_1 and R_2 define a time constant which has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response ($V_A = 3.006\ V_{rms}$).

$$Vo = -AV_A$$

$$\text{where } A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$$

For design purposes, a useful form is R_1/R_2 as a function of A.

$$R_1/R_2 = \frac{4A - 1}{1 - A}$$

(Allowable values for A are those which make R_1/R_2 positive.)

Examples are:

If A = 1 (maximum output), then

$R_1/R_2 = \infty$ or $V(GS_R) = Vo–$; i.e., GS_R is tied to PWRO–

If A = ½, then

$R_1/R_2 = 2$

If A = ¼, (minimum output) then

$R_1/R_2 = 0$ or $V(GS_R) = Vo+$; i.e., GS_R is tied to PWRO+

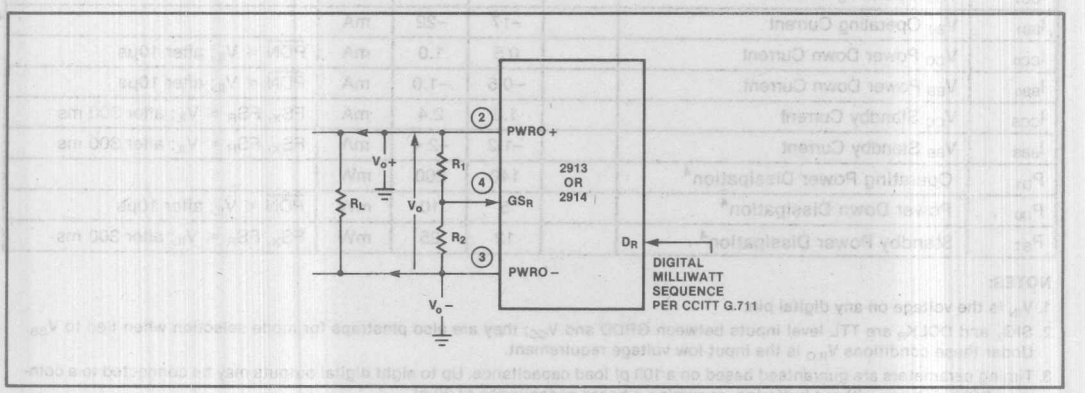


Figure 7. Gain Setting Configuration

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias.....–10°C to +80°C
Storage Temperature.....–65°C to +150°C
V_{CC} and GRDD with Respect to V_{BB}.....–0.3V to 15V
All Input and Output Voltages
with Respect to V_{BB}.....–0.3V to 15V
Power Dissipation.....1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = –5V ±5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)
Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	µA	GRDD ≤ V_{IN} ≤ V_{IL} (Note 1)
I_{IH}	High Level Input Current			10	µA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage, except CLKSEL			0.8	V	
V_{IH}	Input High Voltage, except CLKSEL	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA at D_X, $\overline{TS}_X$ and SIG_R
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 9.6 mA at D_X I_{OH} = 1.2 mA at SIG_R
V_{ILO}	Input Low Voltage, CLKSEL[2]	V_{BB}		V_{BB} +0.5	V	
V_{IIO}	Input Intermediate Voltage, CLKSEL	GRDD −0.5		0.5	V	
V_{IHO}	Input High Voltage, CLKSEL	V_{CC} −0.5		V_{CC}	V	
C_{OX}	Digital Output Capacitance[3]		5		pF	
C_{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC1}	V_{CC} Operating Current		13	17	mA	
I_{BB1}	V_{BB} Operating Current		–17	–22	mA	
I_{CC0}	V_{CC} Power Down Current		0.5	1.0	mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{BB0}	V_{BB} Power Down Current		–0.5	–1.0	mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{CCS}	V_{CC} Standby Current		1.2	2.4	mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
I_{BBS}	V_{BB} Standby Current		–1.2	–2.4	mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
P_{D1}	Operating Power Dissipation[4]		140	200	mW	
P_{D0}	Power Down Dissipation[4]		5	10	mW	$\overline{PDN}$ ≤ V_{IL}; after 10µs
P_{ST}	Standby Power Dissipation[4]		12	25	mW	FS_X, FS_R ≤ V_{IL}; after 300 ms

NOTES:

1. V_{IN} is the voltage on any digital pin.
2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC}; they are also pinstraps for mode selection when tied to V_{BB}. Under these conditions V_{ILO} is the input low voltage requirement.
3. Timing parameters are guaranteed based on a 100 pf load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pf.
4. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, VF_XI+, VF_XI-			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IXI}	Input Resistance, VF_XI+, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-			25	mV	
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	55			dB	$-2.17 \leq V_{IN} \leq 2.17V$
A_{VOL}	DC Open Loop Voltage Gain, GS_X	5000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		1		MHz	
V_{OXI}	Output Voltage Swing GS_X	−2.17		2.17	V	$R_L \geq 10k\Omega$
C_{LXI}	Load Capacitance, GS_X			50	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, PWRO+, PWRO−		75		mV	Relative to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF	
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO−, Single-Ended Connection	−3.06		3.06	V	$R_L \geq 300\Omega$ with zero volt offset
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO−, Balanced Output Connection	−6.12		6.12	V	$R_L \geq 600\Omega$

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.[1] Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration.[2] All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	−0.15	±0.04	+0.15	dBm0	Signal input of 1.064 Vrms μ-law Signal input of 1.068 Vrms A-law T_A = 25°C, V_{BB} = −5V, V_{CC} = +5V
EmW_{TS}	EmW variation with Temperature and supplies	−0.12		+0.12	dB	±5% supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response (Receive gain tolerance)	−0.15	±0.04	+0.15	dBm0	Measure relative to $0TLP_R$. Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz. T_A = 25°C; V_{BB} = −5V, V_{CC} = +5V.
DmW_{TS}	DmW variation with temperature and supplies	−0.08		+0.08	dB	±5% supplies, 0 to 70°C
$0TLP1_X$	Zero Transmission Level Point Transmit Channel (0dBm0) μ-law		+2.76 +1.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBM0) A-law		+2.79 +1.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP1_R$	Zero Transmission Level Point Receive Channel (0dBm0) μ-law		+5.76 +4.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_R$	Zero Transmission Level Point Receive Channel (0dBm0) A-law		+5.79 +4.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω

Notes:
1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms for μlaw.
2. Unity gain input amplifier: GS_X is connected to VF_XI-, Signal input VF_XI+; Maximum gain output amplifier: GS_R is connected to PWRO−, output to PWRO+.

GAIN TRACKING

Reference Level = –10dBm0

Symbol	Parameter	2913-1, 2914-1 Min	2913-1, 2914-1 Max	2913, 2914 Min	2913, 2914 Max	Unit	Test Conditions
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT3_X$	Transmit Gain Tracking Error White Noise Input; A-law		TBD		TBD	dB	CCITT G.712 Method 1
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT3_R$	Receive Gain Tracking Error White Noise Input; A-law		TBD		TBD	dB	CCITT G. 712 Method 1

NOISE

Symbol	Parameter	2913-1, 2914-1 Min	2913-1, 2914-1 Typ	2913-1, 2914-1 Max	2913, 2914 Min	2913, 2914 Typ	2913, 2914 Max	Unit	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted			13			15	dBrnc0	VF_XI+ = GRDA, VF_XI- = GS_X
N_{XC2}	Transmit Noise, C-Message Weighted with Eighth Bit Signaling			16			18	dBrnc0	VF_XI+ = GRDA, VF_XI- = GS_X; 6th frame signaling
N_{XP}	Transmit Noise, Psophometrically Weighted			–77			–75	dBm0p	VF_XI+ = GRDA, VF_XI- = GS_X
N_{RC1}	Receive Noise, C-Message Weighted: Quiet Code			8			11	dBrnc0	D_R = 11111111 Measure at PWRO+
N_{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			9			12	dBrnc0	Input to D_R is zero code with sign bit toggle at 1 kHz rate
N_{RP}	Receive Noise, Psophometrically Weighted			–82			–79	dBm0p	D_R = lowest positive decode level
N_{SF}	Single Frequency Noise End to End Measurement			–50			–50	dBm0	CCITT G.712.4.2
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel		–40			–30		dBC	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel		–40			–30		dBC	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel		–25			–25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel		–25			–25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs			–80			–71	dB	VF_XI+ = 0dBm0, 1.02 kHz, D_R = lowest positive decode level, measure at PWRO+
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs			–80			–71	dB	D_R = 0dBm0, 1.02 kHz, VF_XI+ = GRDA, measure at D_X

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_X$	Transmit Signal to Distortion, A-Law White Noise Input; CCITT G.712-Method 1	TBD				
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_R$	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_R$	Receive Signal To Distortion, A-Law White Noise Input; CCITT G.712-Method 1	TBD				
DP_{X1}	Transmit Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP_{R1}	Receive Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD_1	Intermodulation Distortion, End to End Measurement			−35	dB	CCITT G.712 (7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			−40	dBm0	CCITT G. 712 (9)
D_{AX}	Transmit Absolute Delay		245		μs	Fixed Data Rate. CLK_X = 2.048 MHz; 0 dBm0, 1.02 kHz signal at VF_XI+. Measure at D_X.
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}		170 95 45 105		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz
D_{AR}	Receive Absolute Delay		190		μs	Fixed Data Rate, CLK_R = 2.048 MHz; Digital input is DMW codes. Measure at PWRO+.
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}		45 35 85 110		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, noninverting; maximum gain output.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at VF_XI+
	16.67 Hz			−30	dB	
	50 Hz			−25	dB	
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.10	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−32	dB	

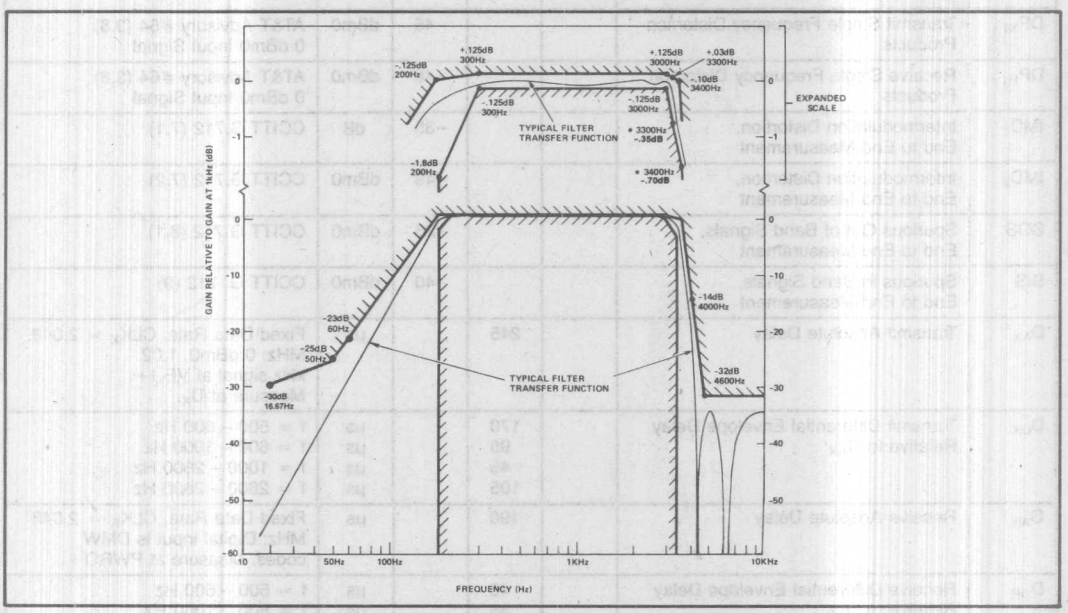


Figure 8. Transmit Channel

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	−0.5		+0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−30	dB	

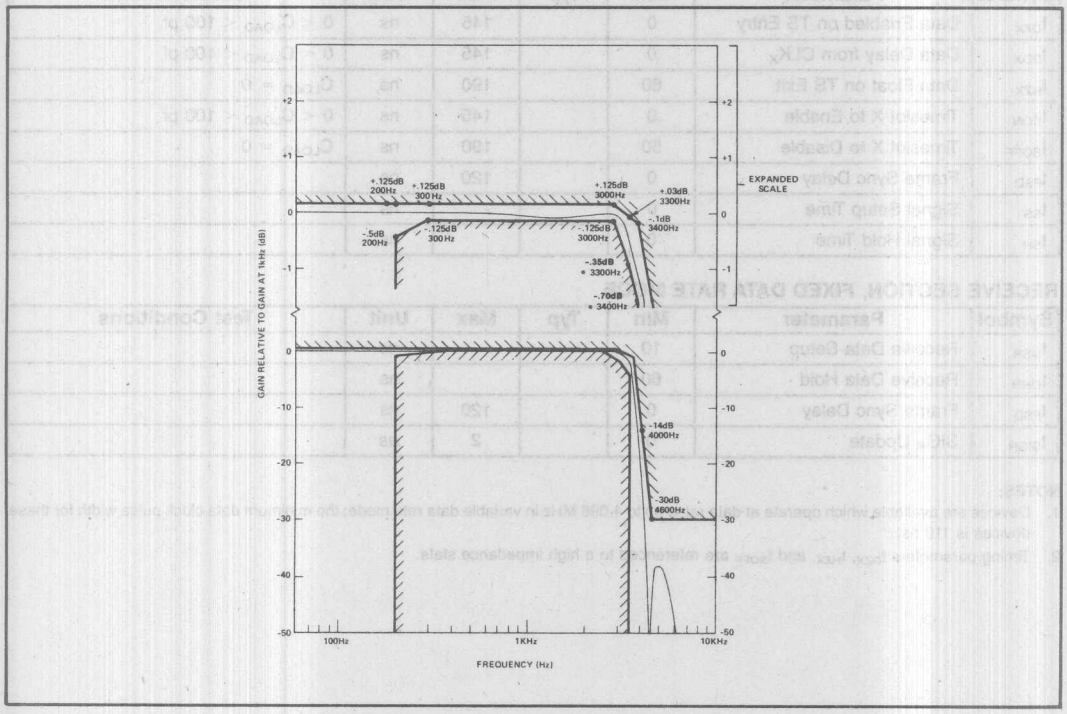


Figure 9. Receive Channel

A.C. CHARACTERISTICS — TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK_X, CLK_R	488			ns	$f_{CLKX} = f_{CLKR} = 2.048$ MHz
t_{CLK}	Clock Pulse Width	195			ns	CLK_X, CLK_R
t_{DCLK}	Data Clock Pulse Width[1]	195			ns	64 kHz $\leq f_{DCLK} \leq$ 2.048 MHz
t_{CDC}	Clock Duty Cycle	40	50	60	%	CLK_X, CLK_R
t_r, t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{DDX}	Data Delay from CLK_X	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{HZX}	Data Float on TS Exit	60		190	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{SOFF}	Timeslot X to Disable	50		190	ns	$C_{LOAD} = 0$
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{SS}	Signal Setup Time	0			ns	
t_{SH}	Signal Hold Time	0			ns	

RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{SIGR}	SIG_R Update	0		2	µs	

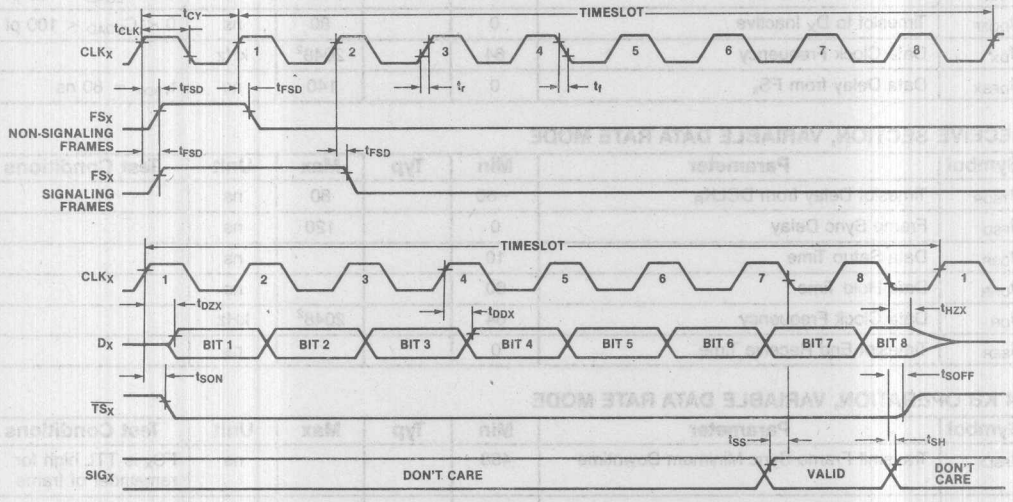
NOTES:

1. Devices are available which operate at data rates up to 4.096 MHz in variable data rate mode; the minimum data clock pulse width for these devices is 110 ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

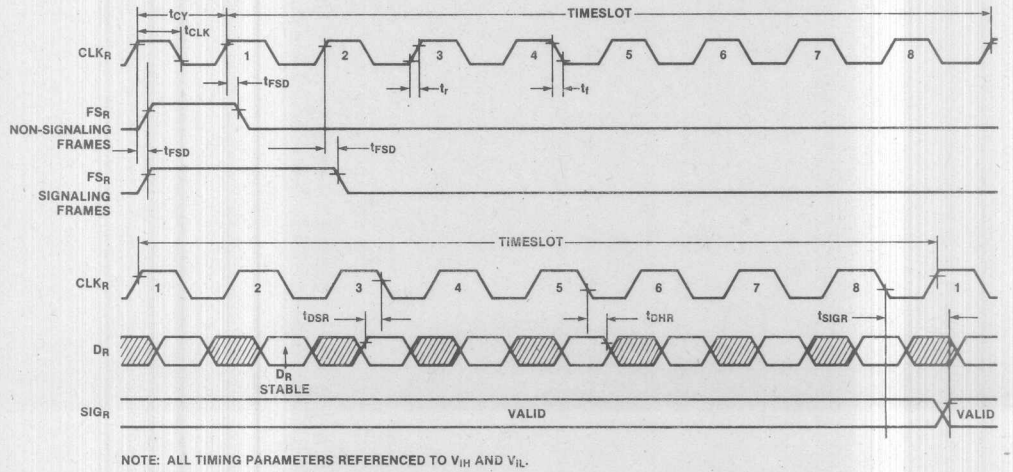
Fixed Data Rate Timing

TRANSMIT TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X$	−80		80	ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
f_{DX}	Data Clock Frequency	64		2048[2]	kHz	
t_{DFSX}	Data Delay from FS_x	0		140	ns	$t_{TSDX} = 80$ ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R$	−80		80	ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
f_{DR}	Data Clock Frequency	64		2048[2]	kHz	
t_{SER}	Timeslot End Receive Time	0			ns	

64 KB OPERATION, VARIABLE DATA RATE MODE

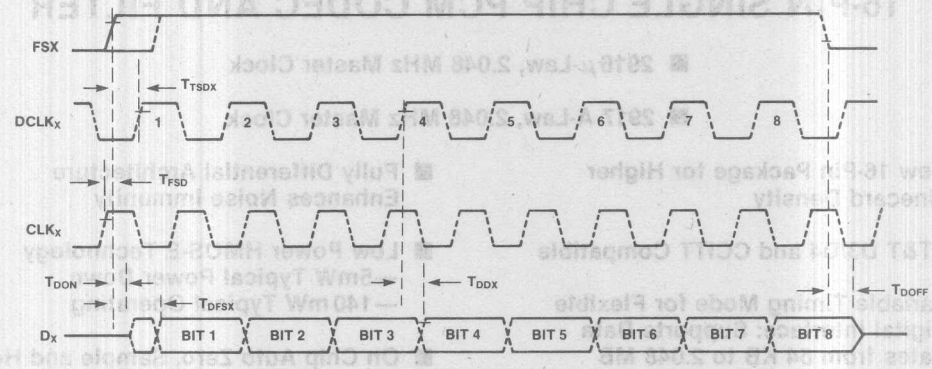
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	µs	

NOTES:

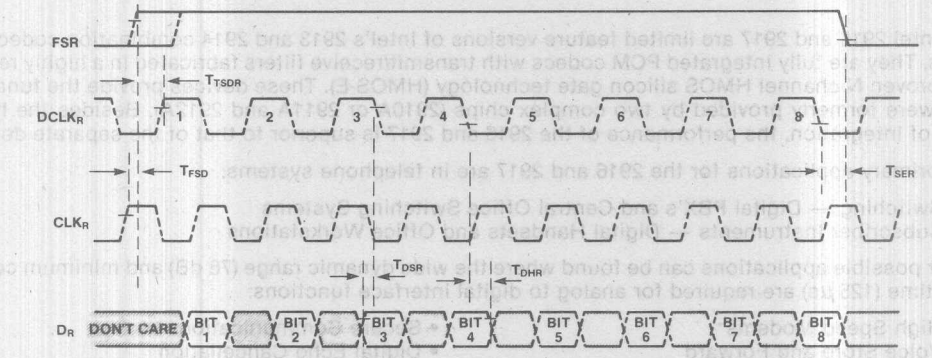
1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Devices are available which operate at data rates up to 4.096 MHz.

VARIABLE DATA RATE TIMING

TRANSMIT TIMING



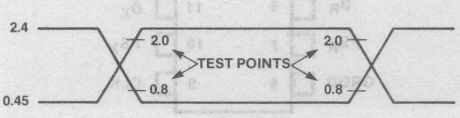
RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DON} AND t_{OFF} WHICH REFERENCE A HIGH IMPEDANCE STATE

A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" and 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

PRELIMINARY

2916 AND 2917
16-PIN SINGLE CHIP PCM CODEC AND FILTER

- **2916 μ-Law, 2.048 MHz Master Clock**
- **2917 A-Law, 2.048 MHz Master Clock**

- **New 16-Pin Package for Higher Linecard Density**
- **AT&T D3/D4 and CCITT Compatible**
- **Variable Timing Mode for Flexible Digital Interface: Supports Data Rates from 64 KB to 2.048 MB**
- **Fixed Timing Mode for Standard 32-Channel Systems: 2.048 MHz Master Clock**
- **Fully Differential Architecture Enhances Noise Immunity**
- **Low Power HMOS-E Technology**
 —5mW Typical Power Down
 —140 mW Typical Operating
- **On Chip Auto Zero, Sample and Hold, and Precision Voltage References**
- **Compatible with Direct Mode Intel 2910A, 2911A, and 2912A Designs**

The Intel 2916 and 2917 are limited feature versions of Intel's 2913 and 2914 combination codec/filter chips. They are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven N-channel HMOS silicon gate technology (HMOS-E). These devices provide the functions that were formerly provided by two complex chips (2910A or 2911A and 2912A). Besides the higher level of integration, the performance of the 2916 and 2917 is superior to that of the separate devices.

The primary applications for the 2916 and 2917 are in telephone systems:

- Switching — Digital PBX's and Central Office Switching Systems
- Subscriber Instruments — Digital Handsets and Office Workstations

Other possible applications can be found where the wide dynamic range (78 dB) and minimum conversion time (125 μs) are required for analog to digital interface functions:

- High Speed Modems
- Voice Store and Forward
- Secure Communications
- Digital Echo Cancellation

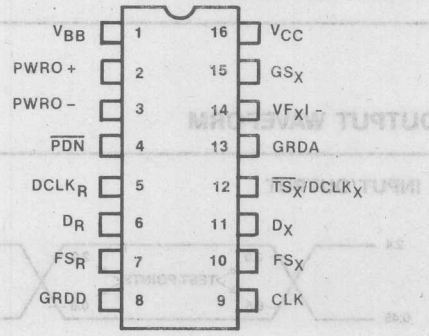


Figure 1. Pin Configurations

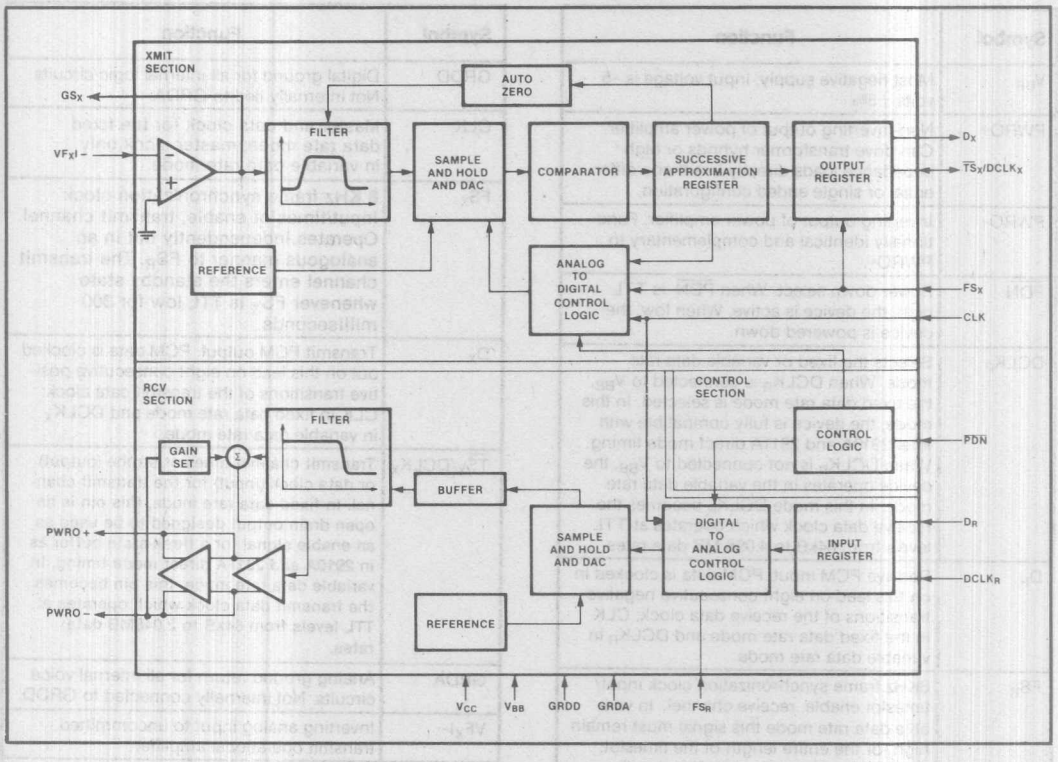


Figure 2. Block Diagram

Table 1. Pin Names

V_{BB}	Power (−5V)	GS_X	Transmit Gain Control
PWRO+, PWRO−	Power Amplifier Outputs	VF_XI-	Analog Input
$\overline{PDN}$	Power Down Select	GRDA	Analog Ground
$DCLK_R$	Receive Variable Data Clock	$\overline{TS_X}$	Timeslot Strobe/Buffer Enable
D_R	Receive PCM Input	$DCLK_X$	Transmit Variable Data Clock
FS_R	Receive Frame Synchronization Clock	D_X	Transmit PCM Output
		FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground		
V_{CC}	Power (+5V)	CLK	Master Clock

Table 2. Pin Description

Symbol	Function
V_{BB}	Most negative supply; input voltage is -5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/timeslot enable, receive channel. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 300 milliseconds.

Symbol	Function
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK	Master and data clock for the fixed data rate mode; master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 300 milliseconds.
D_X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 2.048MB data rates.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 2916 and 2917 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The 2916 and 2917 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500μs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X and $\overline{TS}_X$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the auto-zero circuit settling time.

To enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 20μs after an interruption of CLK.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 2916/2917 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 5 mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 12 mW. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	5 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 10 μs.
Standby Mode	FS_X and FS_R are TTL low	12 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only transmit is on standby	FS_X is TTL low	70 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	110 mW	

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clock CLK, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK serves as the master clock to operate the codec and filter sections and as the bit clock to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency. $\overline{TS}_X$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK. The frequency of CLK must be 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clock CLK, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64 kHz to 2.048 MHz. The master clock is still restricted to 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses a difference in subsurface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04 dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_x) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI-can be either AC or DC coupled. The input op amp can only be used in the inverting mode as shown in Figure 3.

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The 2916 and 2917 specifications meet or exceed digital class

5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 4.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

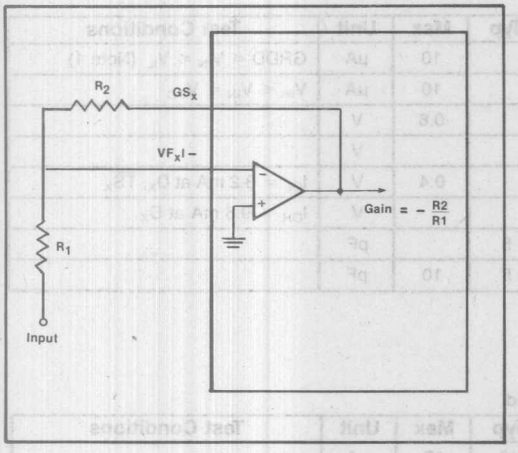


Figure 3. Transmit Filter Gain Adjustment

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications will be within the limits shown in Figure 5.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12 dBM or 600 ohms differentially to a level of 15 dBM.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias −10°C to +80°C
Storage Temperature −65°C to +150°C
V_{CC} and GRDD with Respect to V_{BB} −0.3V to 15V
All Input and Output Voltages with Respect to V_{BB} −0.3V to 15V
Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)

Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	µA	GRDD ≤ V_{IN} ≤ V_{IL} (Note 1)
I_{IH}	High Level Input Current			10	µA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA at D_X, $\overline{TS}_X$
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 9.6 mA at D_X
C_{OX}	Digital Output Capacitance[2]		5		pF	
C_{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC1}	V_{CC} Operating Current		13	17	mA	
I_{BB1}	V_{BB} Operating Current		−17	−22	mA	
I_{CC0}	V_{CC} Power Down Current		0.5	1.0	mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{BB0}	V_{BB} Power Down Current		−0.5	−1.0	mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{CCS}	V_{CC} Standby Current		1.2	2.4	mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
I_{BBS}	V_{BB} Standby Current		−1.2	−2.4	mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
P_{D1}	Operating Power Dissipation[3]		140	200	mW	
P_{D0}	Power Down Dissipation[3]		5	10	mW	$\overline{PDN}$ ≤ V_{IL}; after 10µs
P_{ST}	Standby Power Dissipation[3]		12	25	mW	FS_X, FS_R ≤ V_{IL}; after 300 ms

NOTES:

1. V_{IN} is the voltage on any digital pin.
2. Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pf.
3. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, VF_XI-			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IXI}	Input Resistance, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI-			25	mV	
A_{VOL}	DC Open Loop Voltage Gain, GS_X	5000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		1		MHz	
V_{OXI}	Output Voltage Swing GS_X	−2.17		2.17	V	$R_L \geq 10k\Omega$
C_{LXI}	Load Capacitance, GS_X			50	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, PWRO+, PWRO−		75		mV	Relative to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF	
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO−, Single-Ended Connection	−3.06		3.06	V	$R_L \geq 300\Omega$ with zero volt offset
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO−, Balanced Output Connection	−6.12		6.12	V	$R_L \geq 600\Omega$

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.[1] Input amplifier is set for unity gain,[2] inverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended. All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	−0.15	±0.04	+0.15	dBm0	Signal input of 1.064 Vrms μ-law Signal input of 1.068 Vrms A-law T_A = 25°C, V_{BB} = −5V, V_{CC} = +5V
EmW_{TS}	EmW variation with Temperature and supplies	−0.12		+0.12	dB	±5% supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response (Receive gain tolerance)	−0.15	±0.04	+0.15	dBm0	Measure relative to $0TLP_R$. Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz. T_A = 25°C; V_{BB} = −5V, V_{CC} = +5V.
DmW_{TS}	DmW variation with temperature and supplies	−0.08		+0.08	dB	±5% supplies, 0 to 70°C
$0TLP1_X$	Zero Transmission Level Point Transmit Channel (0dBm0) μ-law		+2.76 +1.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBM0) A-law		+2.79 +1.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP1_R$	Zero Transmission Level Point Receive Channel (0dBm0) μ-law		+5.76 +4.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_R$	Zero Transmission Level Point Receive Channel (0dBm0) A-law		+5.79 +4.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω

NOTES:

1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms (for μlaw).
2. Unity gain input amplifier, signal input VF_xI-.

GAIN TRACKING

Reference Level = –10dBm0

Symbol	Parameter	2916 Min	2916 Max	2917 Min	2917 Max	Unit	Test Conditions
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law		±0.25 ±0.5 ±1.2			dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law				±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT3_X$	Transmit Gain Tracking Error White Noise Input; A-law				TBD	dB	CCITT G.712 Method 1
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law		±0.25 ±0.5 ±1.2			dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law				±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT3_R$	Receive Gain Tracking Error White Noise Input; A-law				TBD	dB	CCITT G. 712 Method 1

NOISE

Symbol	Parameter	2916 Min	2916 Typ	2916 Max	2917 Min	2917 Typ	2917 Max	Unit	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted			15				dBrncO	Unity Gain
N_{XP}	Transmit Noise, Psophometrically Weighted						–75	dBm0p	Unity Gain
N_{RC1}	Receive Noise, C-Message Weighted: Quiet Code			11				dBrncO	D_R = 11111111 Measure at PWRO+
N_{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			12				dBrncO	Input to D_R is zero code with sign bit toggle at 1 kHz rate
N_{RP}	Receive Noise, Psophometrically Weighted						–79	dBm0p	D_R = lowest positive decode level
N_{SF}	Single Frequency Noise End to End Measurement			–50			–50	dBm0	CCITT G.712.4.2
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel		–30			–30		dB	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel		–30			–30		dB	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel		–25			–25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel		–25			–25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs			–71			–71	dB	Input = 0dBm0, Unity Gain, 1.02 kHz, D_R = lowest positive decode level, measure at PWRO+
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs			–71			–71	dB	D_R = 0dBm0, 1.02 kHz, measure at D_X

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2 (2916)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (2917)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_X$	Transmit Signal to Distortion, A-Law White Noise Input; CCITT G.712-Method 1 (2917)	TBD				
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2 (2916)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_R$	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (2917)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_R$	Receive Signal To Distortion, A-Law White Noise Input; CCITT G.712-Method 1 (2917)	TBD				
DP_{X1}	Transmit Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP_{R1}	Receive Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD_1	Intermodulation Distortion, End to End Measurement			−35	dB	CCITT G.712 (7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			−40	dBm0	CCITT G. 712 (9)
D_{AX}	Transmit Absolute Delay		245		μs	Fixed Data Rate. CLK_X = 2.048 MHz; 0 dBm0, 1.02 kHz input Signal, Unity Gain. Measure at D_X.
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}		170 95 45 105		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz
D_{AR}	Receive Absolute Delay		190		μs	Fixed Data Rate, CLK = 2.048 MHz; Digital Input is DMW codes. Measure at PWRO+.
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}		45 35 85 110		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, inverting.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at VF_XI-
	16.67 Hz			−30	dB	
	50 Hz			−25	dB	
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.10	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−32	dB	

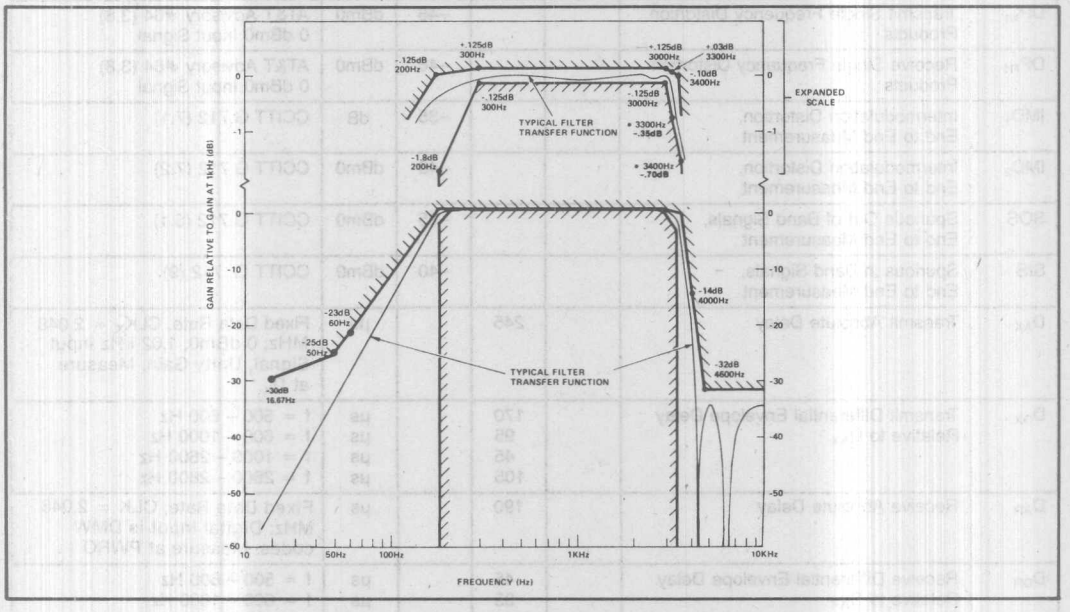


Figure 4. Transmit Channel

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	−0.5		+0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−30	dB	

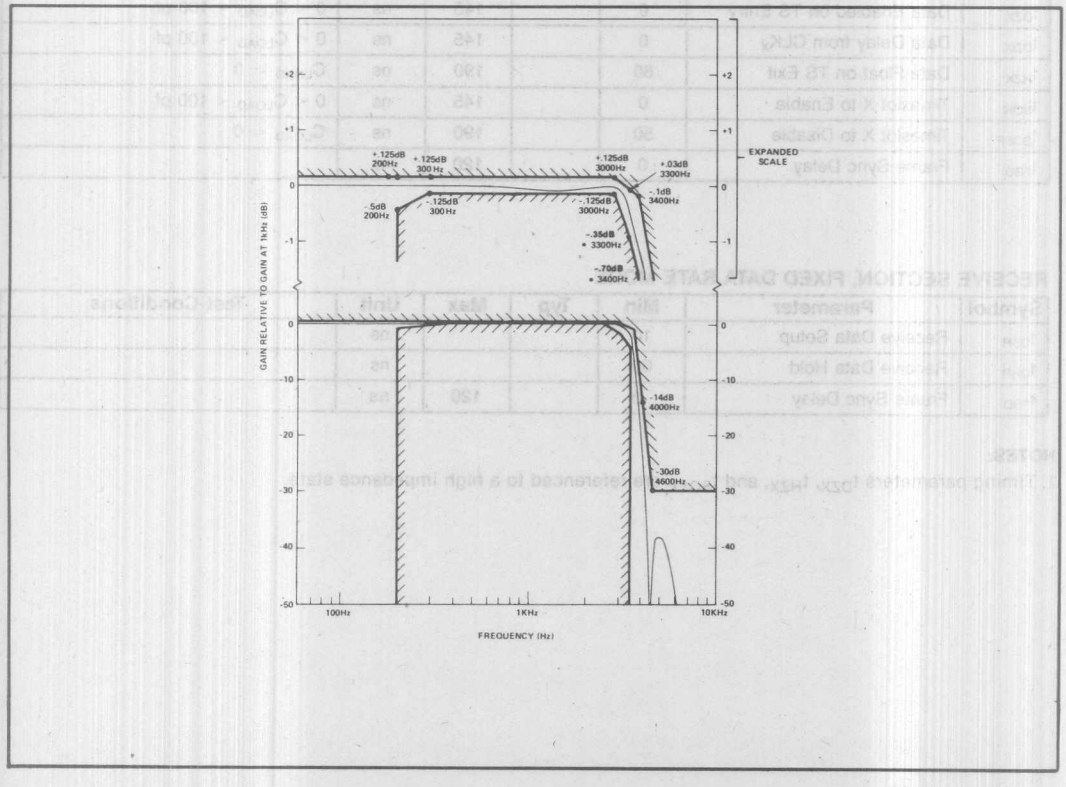


Figure 5. Receive Channel

A.C. CHARACTERISTICS — TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK	488			ns	f_{CLK} = 2.048 MHz
t_{CLK}	Clock Pulse Width	195			ns	CLK
t_{DCLK}	Data Clock Pulse Width	195			ns	64 kHz ≤ f_{DCLK} ≤ 2.048 MHz
t_{CDC}	Clock Duty Cycle	40	50	60	%	CLK
t_r, t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	0 < C_{LOAD} < 100 pf
t_{DDX}	Data Delay from CLK_X	0		145	ns	0 < C_{LOAD} < 100 pf
t_{HZX}	Data Float on TS Exit	60		190	ns	C_{LOAD} = 0
t_{SON}	Timeslot X to Enable	0		145	ns	0 < C_{LOAD} < 100 pf
t_{SOFF}	Timeslot X to Disable	50		190	ns	C_{LOAD} = 0
t_{FSD}	Frame Sync Delay	0		120	ns	

RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	0		120	ns	

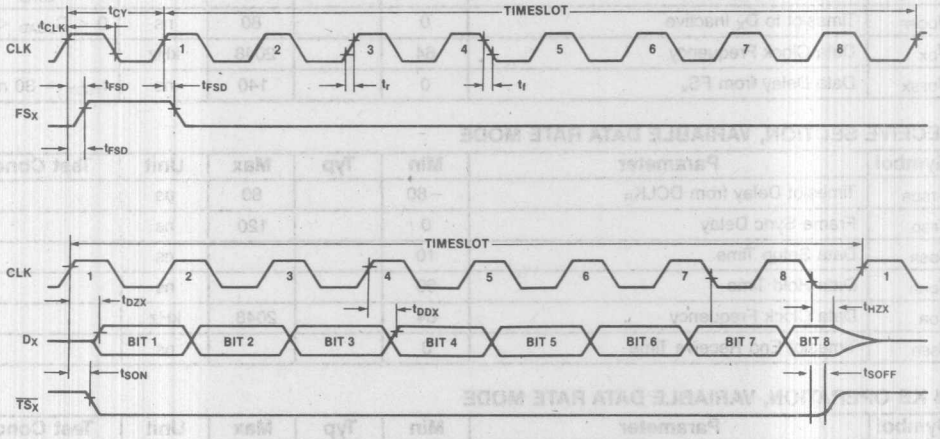
NOTES:

1. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

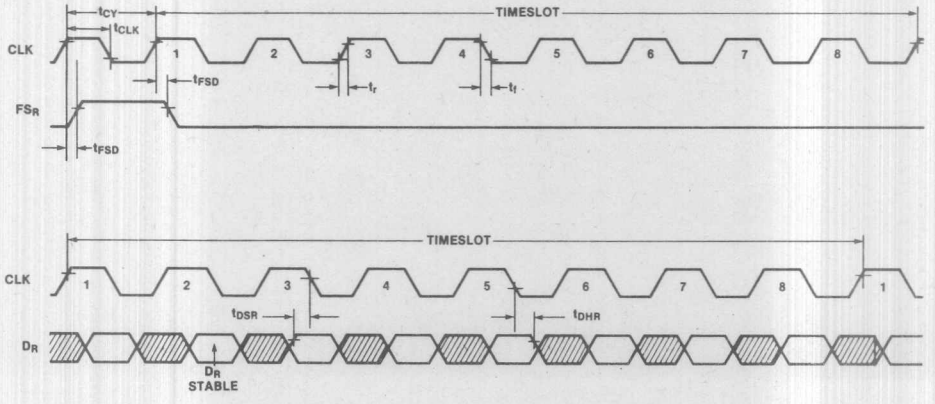
Fixed Data Rate Timing

TRANSMIT TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X$	−80		80	ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
f_{DX}	Data Clock Frequency	64		2048	kHz	
t_{DFSX}	Data Delay from FS_x	0		140	ns	t_{TSDX} = 80 ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R$	−80		80	ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
f_{DR}	Data Clock Frequency	64		2048	kHz	
t_{SER}	Timeslot End Receive Time	0			ns	

64 KB OPERATION, VARIABLE DATA RATE MODE

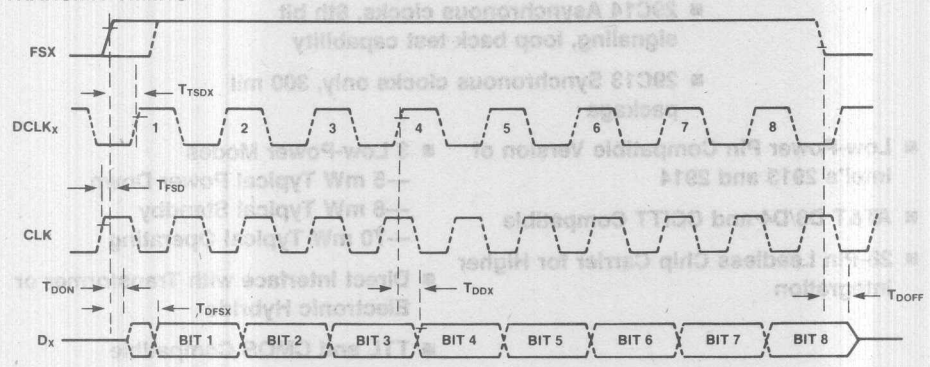
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	µs	

NOTES:

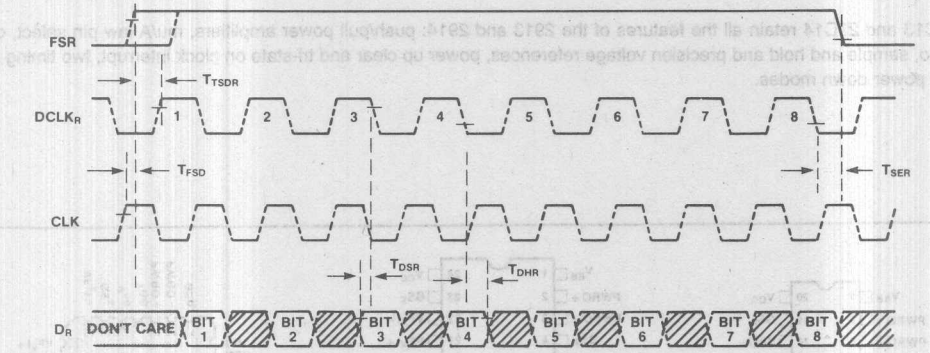
1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.

VARIABLE DATA RATE TIMING

TRANSMIT TIMING



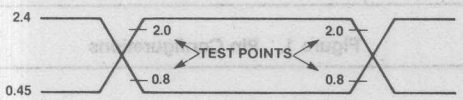
RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DON} AND t_{OFF} WHICH REFERENCE A HIGH IMPEDANCE STATE

A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" and 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

29C13 AND 29C14
CHMOS COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- **29C14 Asynchronous clocks, 8th bit signaling, loop back test capability**
- **29C13 Synchronous clocks only, 300 mil package**
- **Low-Power Pin Compatible Version of Intel's 2913 and 2914**
- **AT&T D3/D4 and CCITT Compatible**
- **28-Pin Leadless Chip Carrier for Higher Integration**
- **3 Low-Power Modes**
 —5 mW Typical Power Down
 —8 mW Typical Standby
 —70 mW Typical Operating
- **Direct Interface with Transformer or Electronic Hybrids**
- **TTL and CMOS Compatible**

Intel's 29C13 and 29C14 are CHMOS versions of Intel's HMOS 2913 and 2914 family members. CHMOS is a technology built on HMOS-II, thus realizing the high performance and density obtained in that process while achieving the low power consumption typical of CMOS circuits.

The 29C13 and 29C14 retain all the features of the 2913 and 2914: push/pull power amplifiers, mu/A law pin select, on-chip auto zero, sample and hold and precision voltage references, power up clear and tri-state on clock interrupt, two timing modes and two power down modes.

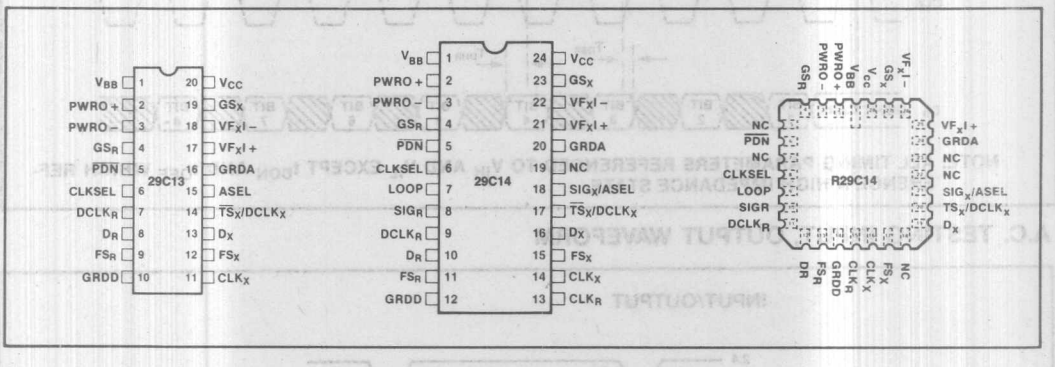


Figure 1. Pin Configurations

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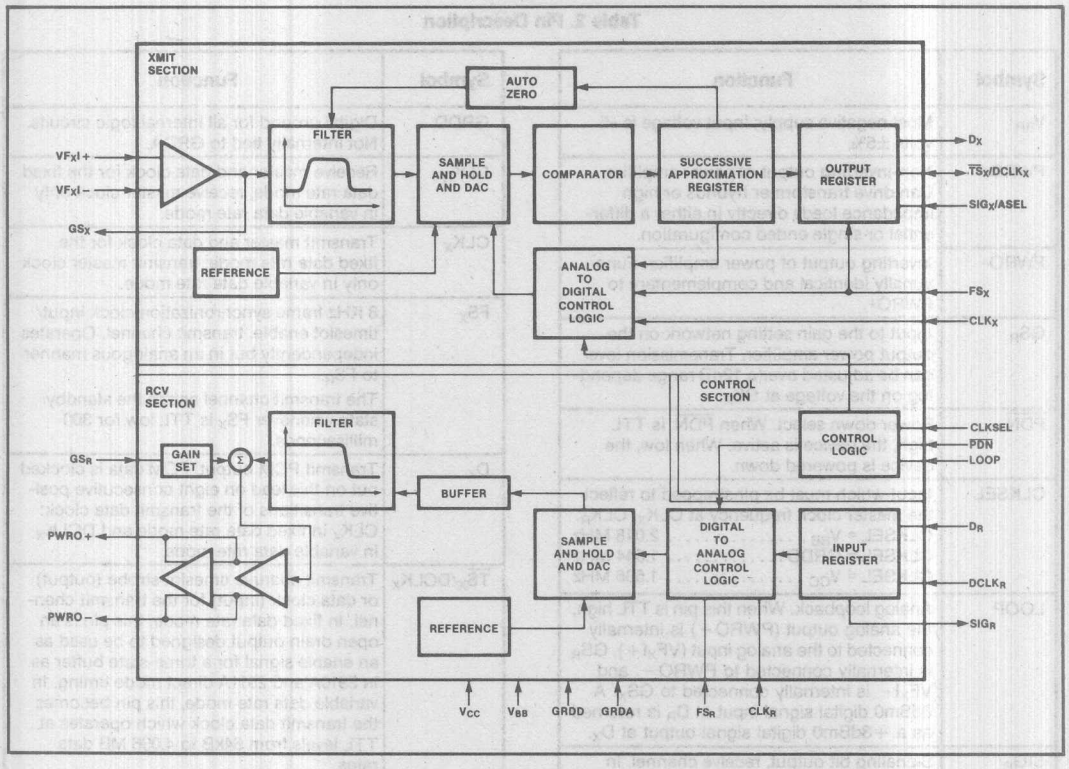


Figure 2. Block Diagram

Table 1. Pin Names

V_{BB}	Power (-5V)	GS_X	Transmit Gain Control
PWRO+, PWRO−	Power Amplifier Outputs	VF_XI-, VF_XI+	Analog Inputs
GS_R	Receive Gain Control	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG_X	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-law Select
SIG_R	Receive Signaling Bit Output	$\overline{TS_X}$	Timeslot Strobe/Buffer Enable
$DCLK_R$	Receive Variable Data Clock	$DCLK_X$	Transmit Variable Data Clock
D_R	Receive PCM Input	D_X	Transmit PCM Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

Table 2. Pin Description

Symbol	Function
V_{BB}	Most negative supply; input voltage is -5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO–	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} 2.048 MHz CLKSEL = GRDD 1.544 MHz CLKSEL = V_{CC} 1.536 MHz
LOOP	Analog loopback. When this pin is TTL high, the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO–, and VF_XI- is internally connected to GS_X. A 0dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
SIG_R	Signaling bit output, receive channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/ timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 300 milliseconds.

Symbol	Function
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/ timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 300 milliseconds.
D_X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
SIG_X/ASEL	A dual purpose pin. When connected to V_{BB}, A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	No connect
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 29C13 and 29C14 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

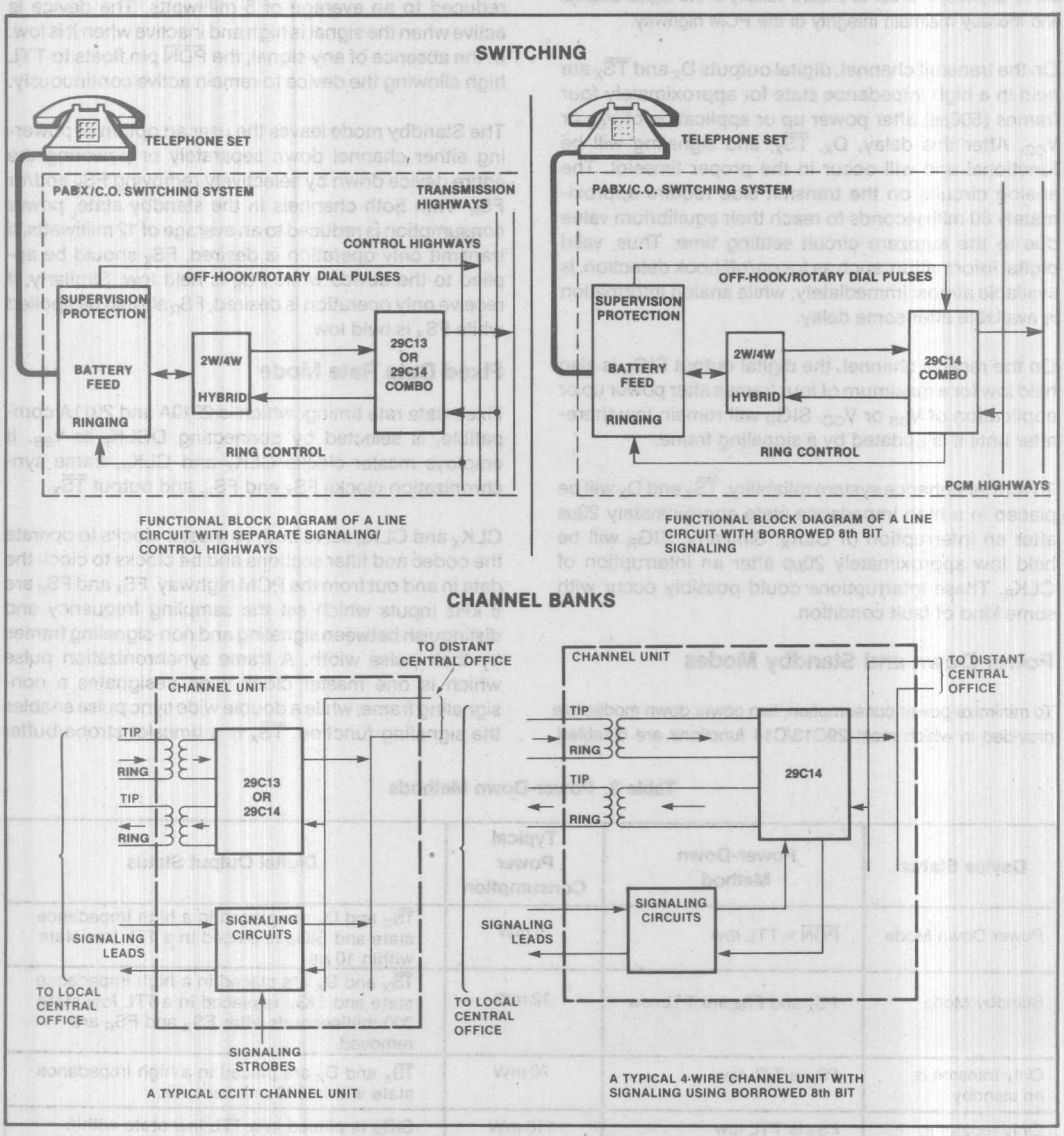


Figure 3. Typical Line Terminations

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The 29C13 and 29C14 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500μs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X, $\overline{TS}_X$, and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit settling time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 20μs after an interruption of CLK_X. Similarly, SIG_R will be held low approximately 20μs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 29C13/C14 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 5 milliwatts. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 12 milliwatts. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clocks CLK_X and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. $\overline{TS}_X$ is a timeslot strobe/buffer

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	5 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 μs
Standby Mode	FS_X and FS_R are TTL low	12 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 300 milliseconds after FS_X and FS_R are removed.
Only transmit is on standby	FS_X is TTL low	70 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	110 mW	SIG_R is placed in a TTL low state within 300 milliseconds.

enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544, or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the 29C14, synchronous in the case of the 29C13 from 64 kHz to 4.096 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125μs frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Signaling

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R = V_{BB}$). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in Figure 4.

Asynchronous Operation

The 29C14 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry,

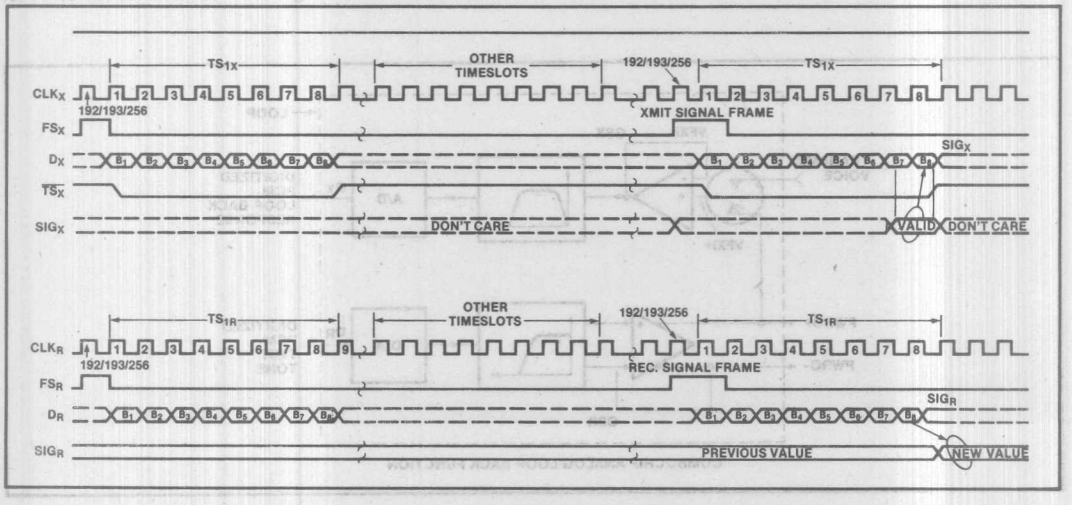


Figure 4. Signaling Timing (Used Only with Fixed Data Rate Mode)

the design of the Intel 29C13/C14 combochip includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in variable data rate mode the rising edge of CLK_X must occur within t_{FSD} nanoseconds before the rise of FS_X, while the leading edge of $DCLK_X$ must occur within t_{TSDX} nanoseconds of the rise of FS_X. Thus, CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagrams, page 18). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

Analog Loopback

A distinctive feature of the 29C14 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in Figure 5, when LOOP is TTL high the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO−, and VF_XI- is internally connected to GS_X.

With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a 0 dBm0 code sent into D_R will emerge from D_X as a +3dBm0 code, an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses a difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

Conversion Laws

The 29C13 and 29C14 are designed to operate in both μ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for

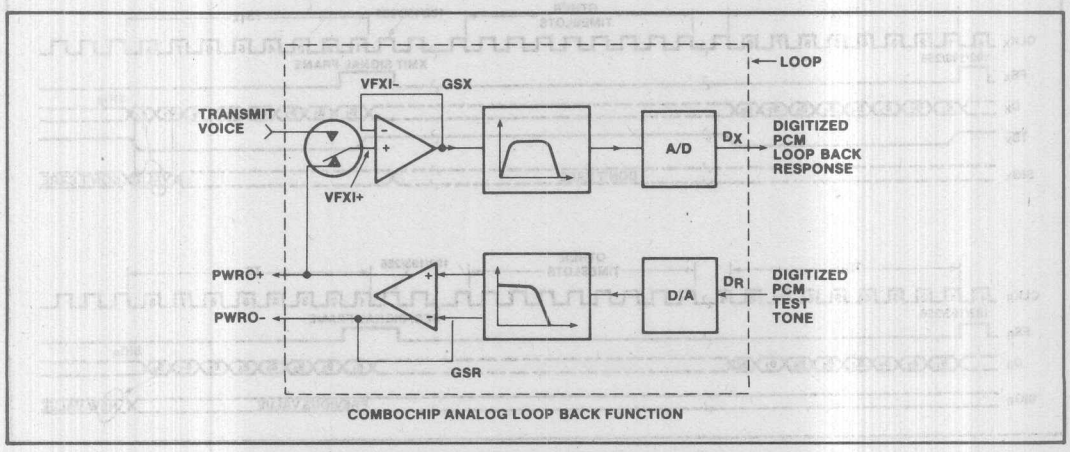


Figure 5. Simplified Block Diagram of 29C14 Combochip in the Analog Loopback Configuration

μ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If μ = 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB of the PCM output in signaling frames.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see Figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The

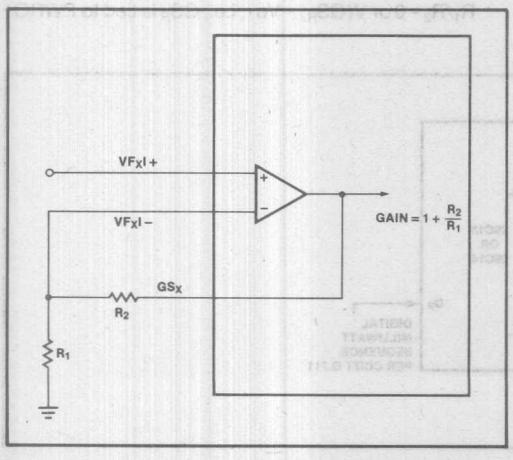


Figure 6. Transmit Filter Gain Adjustment

29C13 and 29C14 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown on pages 14 and 15.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications are shown on pages 14 and 15.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to

GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12 dBM or 600 ohms differentially to a level of 15 dBM.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO–, the receive level is maximized; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and –12 dB as GS_R is interpolated (with a potentiometer) between PWRO+ and PWRO–. The use of the output gain set is illustrated in Figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET: DESIGN CONSIDERATIONS

(Refer to Figure 7.)

PWRO+ and PWRO– are low impedance complementary outputs. The voltages at the nodes are:

Vo+ at PWRO+

Vo– at PWRO–

Vo = Vo+ – Vo– (total differential response)

R_1 and R_2 are a gain setting resistor network with the center tap connected to the GS_R input.

A value greater than 10K ohms and less than 100K for $R_1 + R_2$ is recommended because:

(a) The parallel combination of $R_1 + R_2$ and R_L sets the total loading.

(b) The total capacitance at the GS_R input and the parallel combination of R_1 and R_2 define a time constant which has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response ($V_A = 3.006\ V_{rms}$).

$$Vo = -AV_A$$

$$\text{where } A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$$

For design purposes, a useful form is R_1/R_2 as a function of A.

$$R_1/R_2 = \frac{4A - 1}{1 - A}$$

(Allowable values for A are those which make R_1/R_2 positive.)

Examples are:

If A = 1 (maximum output), then

$R_1/R_2 = \infty$ or $V(GS_R) = Vo–$; i.e., GS_R is tied to PWRO–

If A = ½, then

$R_1/R_2 = 2$

If A = ¼, (minimum output) then

$R_1/R_2 = 0$ or $V(GS_R) = Vo+$; i.e., GS_R is tied to PWRO+

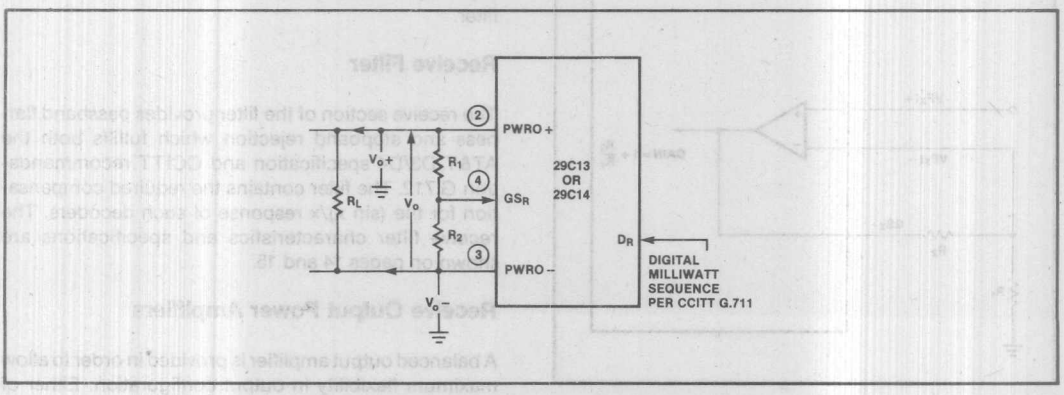


Figure 7. Gain Setting Configuration

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias.....–10°C to +80°C
Storage Temperature.....–65°C to +150°C
V_{CC} and GRDD with Respect to V_{BB}.....–0.3V to 15V
All Input and Output Voltages
with Respect to V_{BB}.....–0.3V to 15V
Power Dissipation.....1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = –5V ±5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)
Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	µA	GRDD ≤ V_{IN} ≤ V_{IL} (Note 1)
I_{IH}	High Level Input Current			10	µA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage, except CLKSEL			0.8	V	
V_{IH}	Input High Voltage, except CLKSEL	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA at D_X, $\overline{TS_X}$ and SIG_R
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 9.6 mA at D_X I_{OH} = 1.2 mA at SIG_R
V_{ILO}	Input Low Voltage, CLKSEL[2]	V_{BB}		V_{BB} +0.5	V	
V_{IIO}	Input Intermediate Voltage, CLKSEL	GRDD −0.5		0.5	V	
V_{IHO}	Input High Voltage, CLKSEL	V_{CC} −0.5		V_{CC}	V	
C_{OX}	Digital Output Capacitance[3]		5		pF	
C_{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC1}	V_{CC} Operating Current		6.8		mA	
I_{BB1}	V_{BB} Operating Current		7.2		mA	
I_{CC0}	V_{CC} Power Down Current		0.5		mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{BB0}	V_{BB} Power Down Current		0.5		mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{CCS}	V_{CC} Standby Current		0.8		mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
I_{BBS}	V_{BB} Standby Current		0.8		mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
P_{D1}	Operating Power Dissipation[4]		70		mW	
P_{D0}	Power Down Dissipation[4]		5		mW	$\overline{PDN}$ ≤ V_{IL}; after 10µs
P_{ST}	Standby Power Dissipation[4]		8		mW	FS_X, FS_R ≤ V_{IL}; after 300 ms

NOTES:

1. V_{IN} is the voltage on any digital pin.
2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC}; they are also pinstraps for mode selection when tied to V_{BB}. Under these conditions V_{ILO} is the input low voltage requirement.
3. Timing parameters are guaranteed based on a 100 pf load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pf.
4. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, VF_XI+, VF_XI-			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IXI}	Input Resistance, VF_XI+, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-			25	mV	
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	55			dB	$-2.17 \leq V_{IN} \leq 2.17V$
A_{VOL}	DC Open Loop Voltage Gain, GS_X	5000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		1		MHz	
V_{OXI}	Output Voltage Swing GS_X	−2.17		2.17	V	$R_L \geq 10k\Omega$
C_{LXI}	Load Capacitance, GS_X			50	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, PWRO+, PWRO−		75		mV	Relative to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF	
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO−, Single-Ended Connection	−3.06		3.06	V	$R_L \geq 300\Omega$ with zero volt offset
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO−, Balanced Output Connection	−6.12		6.12	V	$R_L \geq 600\Omega$

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.[1] Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration.[2] All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	−0.15	±0.04	+0.15	dBm0	Signal input of 1.064 Vrms μ-law Signal input of 1.068 Vrms A-law T_A = 25°C, V_{BB} = −5V, V_{CC} = +5V
EmW_{TS}	EmW variation with Temperature and supplies	−0.12		+0.12	dB	±5% supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response (Receive gain tolerance)	−0.15	±0.04	+0.15	dBm0	Measure relative to $0TLP_R$. Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz. T_A = 25°C; V_{BB} = −5V, V_{CC} = +5V.
DmW_{TS}	DmW variation with temperature and supplies	−0.08		+0.08	dB	±5% supplies, 0 to 70°C
$0TLP1_X$	Zero Transmission Level Point Transmit Channel (0dBm0) μ-law		+2.76 +1.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBM0) A-law		+2.79 +1.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP1_R$	Zero Transmission Level Point Receive Channel (0dBm0) μ-law		+5.76 +4.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_R$	Zero Transmission Level Point Receive Channel (0dBm0) A-law		+5.79 +4.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω

Notes:
1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms for μlaw.
2. Unity gain input amplifier: GS_X is connected to VF_XI-, Signal input VF_XI+; Maximum gain output amplifier: GS_R is connected to PWRO−, output to PWRO+.

GAIN TRACKING

Reference Level = –10dBm0

Symbol	Parameter	29C13-1, 29C14-1 Min	29C13-1, 29C14-1 Max	29C13, 29C14 Min	29C13, 29C14 Max	Unit	Test Conditions
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT3_X$	Transmit Gain Tracking Error White Noise Input; A-law		TBD		TBD	dB	CCITT G.712 Method 1
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law		±0.2 ±0.3 ±0.65		±0.25 ±0.5 ±1.2	dB dB dB	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0
$GT3_R$	Receive Gain Tracking Error White Noise Input; A-law		TBD		TBD	dB	CCITT G. 712 Method 1

NOISE

Symbol	Parameter	29C13-1, 29C14-1 Min	29C13-1, 29C14-1 Typ	29C13-1, 29C14-1 Max	29C13, 29C14 Min	29C13, 29C14 Typ	29C13, 29C14 Max	Unit	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted			13			15	dBrnc0	VF_XI+ = GRDA, VF_XI- = GS_X
N_{XC2}	Transmit Noise, C-Message Weighted with Eighth Bit Signaling			16			18	dBrnc0	VF_XI+ = GRDA, VF_XI- = GS_X; 6th frame signaling
N_{XP}	Transmit Noise, Psophometrically Weighted			–77			–75	dBm0p	VF_XI+ = GRDA, VF_XI- = GS_X
N_{RC1}	Receive Noise, C-Message Weighted: Quiet Code			8			11	dBrnc0	D_R = 11111111 Measure at PWRO+
N_{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			9			12	dBrnc0	Input to D_R is zero code with sign bit toggle at 1 kHz rate
N_{RP}	Receive Noise, Psophometrically Weighted			–82			–79	dBm0p	D_R = lowest positive decode level
N_{SF}	Single Frequency Noise End to End Measurement			–50			–50	dBm0	CCITT G.712.4.2
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel		–40			–30		dBC	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel		–40			–30		dBC	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel		–25			–25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel		–25			–25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs			–80			–71	dB	VF_XI+ = 0dBm0, 1.02 kHz, D_R = lowest positive decode level, measure at PWRO+
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs			–80			–71	dB	D_R = 0dBm0, 1.02 kHz, VF_XI+ = GRDA, measure at D_X

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_X$	Transmit Signal to Distortion, A-Law White Noise Input; CCITT G.712-Method 1	TBD				
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_R$	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_R$	Receive Signal To Distortion, A-Law White Noise Input; CCITT G.712-Method 1	TBD				
DP_{X1}	Transmit Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP_{R1}	Receive Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD_1	Intermodulation Distortion, End to End Measurement			−35	dB	CCITT G.712 (7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			−40	dBm0	CCITT G. 712 (9)
D_{AX}	Transmit Absolute Delay		245		μs	Fixed Data Rate. CLK_X = 2.048 MHz; 0 dBm0, 1.02 kHz signal at VF_XI+. Measure at D_X.
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}		170 95 45 105		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz
D_{AR}	Receive Absolute Delay		190		μs	Fixed Data Rate, CLK_R = 2.048 MHz; Digital input is DMW codes. Measure at PWRO+.
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}		45 35 85 110		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, noninverting; maximum gain output.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at VF_XI+
	16.67 Hz			−30	dB	
	50 Hz			−25	dB	
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.10	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−32	dB	

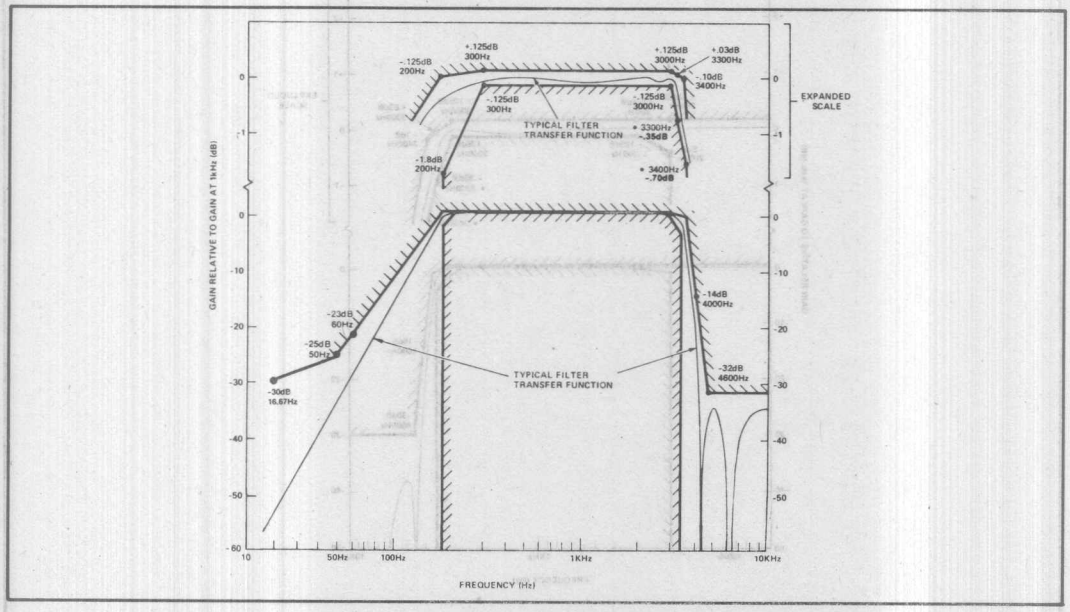


Figure 8. Transmit Channel

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	−0.5		+0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−30	dB	

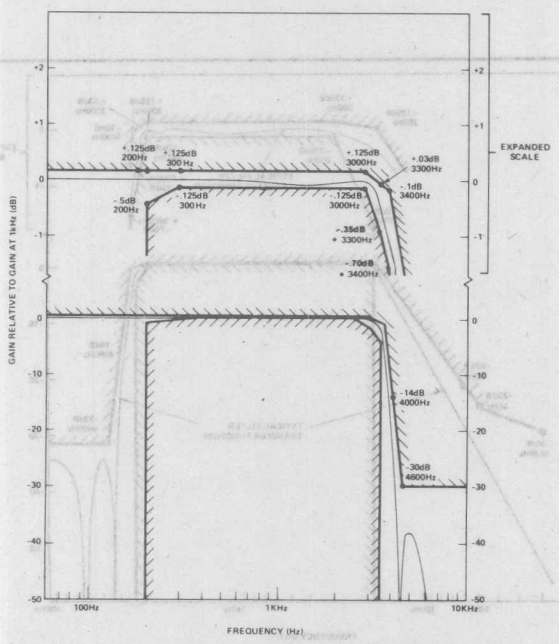


Figure 9. Receive Channel

A.C. CHARACTERISTICS — TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK_X, CLK_R	488			ns	$f_{CLKX} = f_{CLKR} = 2.048$ MHz
t_{CLK}	Clock Pulse Width	195			ns	CLK_X, CLK_R
t_{DCLK}	Data Clock Pulse Width[1]	195			ns	64 kHz $\leq f_{DCLK} \leq$ 2.048 MHz
t_{CDC}	Clock Duty Cycle	40	50	60	%	CLK_X, CLK_R
t_r, t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{DDX}	Data Delay from CLK_X	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{HZX}	Data Float on TS Exit	60		190	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{SOFF}	Timeslot X to Disable	50		190	ns	$C_{LOAD} = 0$
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{SS}	Signal Setup Time	0			ns	
t_{SH}	Signal Hold Time	0			ns	

RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{SIGR}	SIG_R Update	0		2	µs	

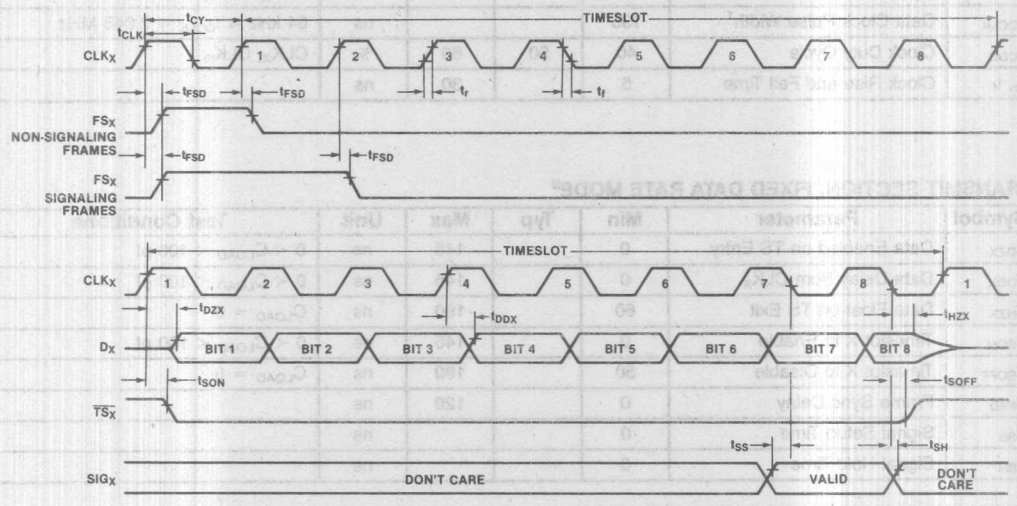
NOTES:

1. Devices are available which operate at data rates up to 4.096 MHz in variable data rate mode; the minimum data clock pulse width for these devices is 110 ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

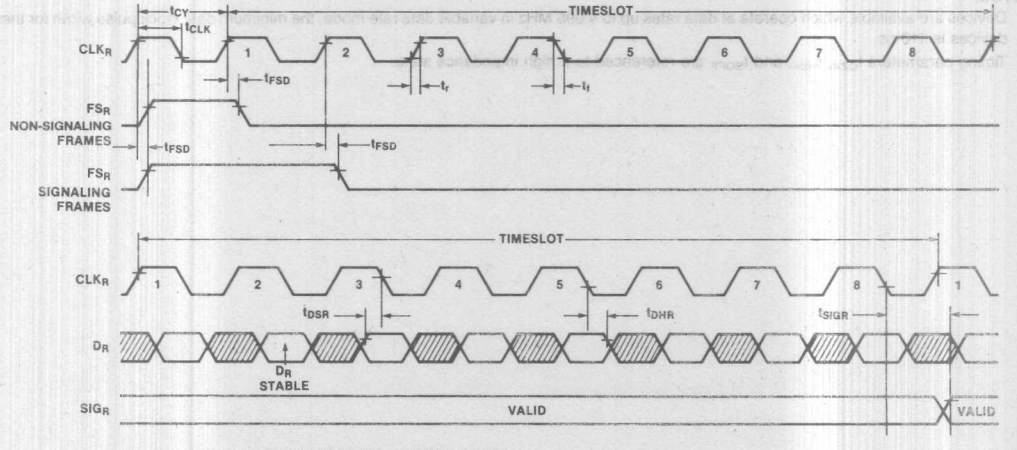
Fixed Data Rate Timing

TRANSMIT TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X$	−80		80	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
f_{DX}	Data Clock Frequency	64		2048[2]	kHz	
t_{DFSX}	Data Delay from FS_x	0		140	ns	t_{TSDX} = 80 ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R$	−80		80	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
f_{DR}	Data Clock Frequency	64		2048[2]	kHz	
t_{SER}	Timeslot End Receive Time	0			ns	

64 KB OPERATION, VARIABLE DATA RATE MODE

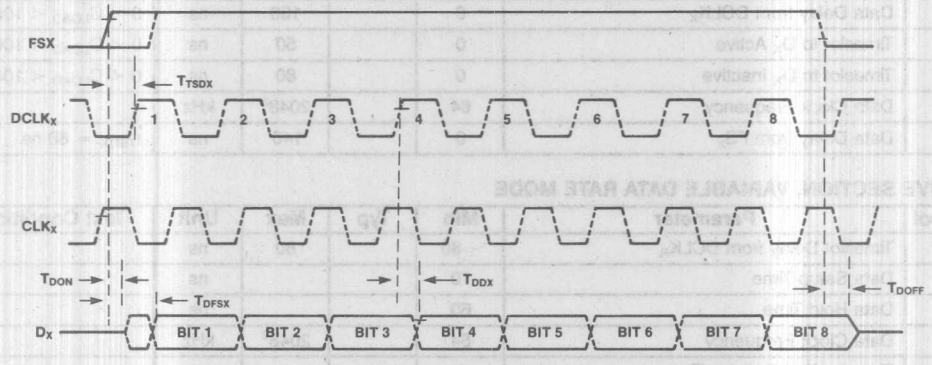
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	µs	

NOTES:

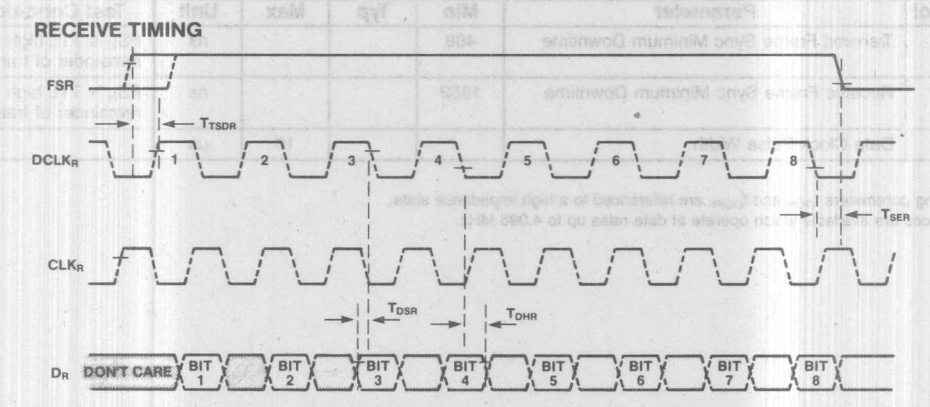
1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Devices are available which operate at data rates up to 4.096 MHz.

VARIABLE DATA RATE TIMING

TRANSMIT TIMING



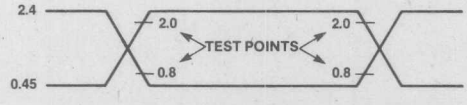
RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DON} AND t_{OFF} WHICH REFERENCE A HIGH IMPEDANCE STATE

A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" and 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

29C16 AND 29C17
16 PIN CHMOS SINGLE-CHIP PCM CODEC AND FILTER

- 29C16 μ-Law, 2.048 MHz Master Clock
- 29C17 A-Law, 2.048 MHz Master Clock

- Low-Power Pin Compatible Version of Intel's 2916 and 2917
- AT&T D3/D4 and CCITT Compatible
- 16-Pin Package for Higher Linecard Densities
- Ideal for Digital Handset Applications
- 3 Low-Power Modes
 - 5mW Typical Power Down
 - 8mW Typical Standby
 - 70mW Typical Operating
- TTL and CMOS Compatible
- Two Timing Modes
 - 64 KHz to 2 MHz Variable
 - 2 MHz Direct

Intel's 29C16 and 29C17 are CHMOS versions of Intel's NMOS 2916 and 2917 family members. CHMOS is a technology built on HMOS-II, thus realizing the high performance and density obtained in that process while achieving the low power consumption typical of CMOS circuits.

The 29C16 and 29C17 are limited feature versions of the 29C13 and 29C14. The inherent low-power and small package size make these devices ideal for digital handset and cellular telephones where small size and low power are especially desirable.

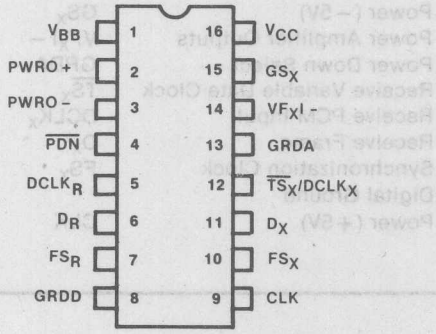


Figure 1. Pin Configurations

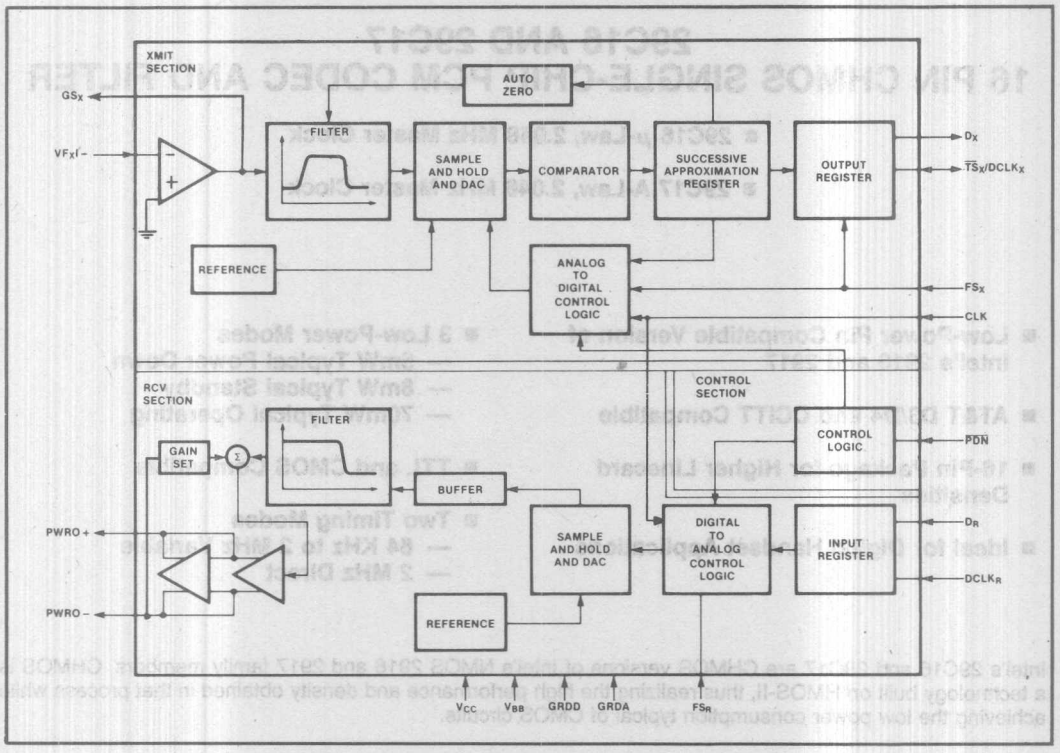


Figure 2. Block Diagram

Table 1. Pin Names

V_{BB}	Power (−5V)	GS_X	Transmit Gain Control
PWRO+, PWRO−	Power Amplifier Outputs	VF_XI-	Analog Input
$\overline{PDN}$	Power Down Select	GRDA	Analog Ground
$DCLK_R$	Receive Variable Data Clock	$\overline{TS_X}$	Timeslot Strobe/Buffer Enable
D_R	Receive PCM Input	$DCLK_X$	Transmit Variable Data Clock
FS_R	Receive Frame Synchronization Clock	D_X	Transmit PCM Output
		FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground		
V_{CC}	Power (+5V)	CLK	Master Clock

Table 2. Pin Description

Symbol	Function
V_{BB}	Most negative supply; input voltage is -5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock, CLK in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/timeslot enable, receive channel. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 300 milliseconds.

Symbol	Function
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK	Master and data clock for the fixed data rate mode; master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 300 milliseconds.
D_X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock; CLK in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS}_X/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 2.048MB data rates.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 29C16 and 29C17 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The 29C16 and 29C17 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500μs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X and $\overline{TS}_X$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the auto-zero circuit settling time.

To enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 20μs after an interruption of CLK.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 29C16/C17 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 5 mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 12 mW. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	5 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 10 μs.
Standby Mode	FS_X and FS_R are TTL low	12 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only transmit is on standby	FS_X is TTL low	70 mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	110 mW	

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clock CLK, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK serves as the master clock to operate the codec and filter sections and as the bit clock to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency. $\overline{TS}_X$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK. The frequency of CLK must be 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clock CLK, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64 kHz to 2.048 MHz. The master clock is still restricted to 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses a difference in subsurface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04 dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_x) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI-can be either AC or DC coupled. The input op amp can only be used in the inverting mode as shown in Figure 3.

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The 29C16 and 29C17 specifications meet or exceed digital class 5 central

office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 4.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

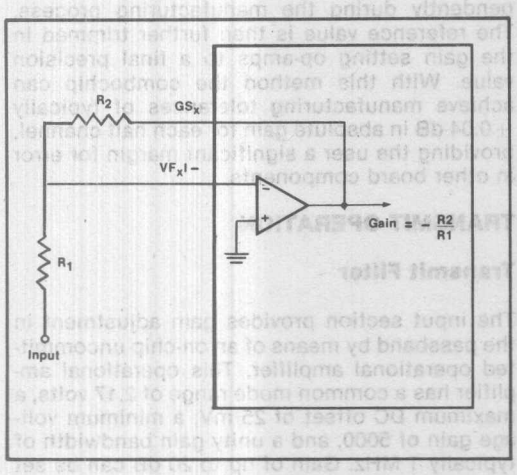


Figure 3. Transmit Filter Gain Adjustment

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications will be within the limits shown in Figure 5.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12 dBM or 600 ohms differentially to a level of 15 dBM.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias −10°C to +80°C
Storage Temperature −65°C to +150°C
V_{CC} and GRDD with Respect to V_{BB} −0.3V to 15V
All Input and Output Voltages with Respect to V_{BB} −0.3V to 15V
Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)
Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	µA	GRDD ≤ V_{IN} ≤ V_{IL} (Note 1)
I_{IH}	High Level Input Current			10	µA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA at D_X, $\overline{TS}_X$
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 9.6 mA at D_X
C_{OX}	Digital Output Capacitance[2]		5		pF	
C_{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC1}	V_{CC} Operating Current		6.8		mA	
I_{BB1}	V_{BB} Operating Current		7.2		mA	
I_{CC0}	V_{CC} Power Down Current		0.5		mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{BB0}	V_{BB} Power Down Current		0.5		mA	$\overline{PDN}$ ≤ V_{IL}; after 10µs
I_{CCS}	V_{CC} Standby Current		0.8		mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
I_{BBS}	V_{BB} Standby Current		0.8		mA	FS_X, FS_R ≤ V_{IL}; after 300 ms
P_{D1}	Operating Power Dissipation[3]		70		mW	
P_{D0}	Power Down Dissipation[3]		5		mW	$\overline{PDN}$ ≤ V_{IL}; after 10µs
P_{ST}	Standby Power Dissipation[3]		8		mW	FS_X, FS_R ≤ V_{IL}; after 300 ms

NOTES:

1. V_{IN} is the voltage on any digital pin.
2. Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pf.
3. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, VF_XI-			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IXI}	Input Resistance, VF_XI-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI-			25	mV	
A_{VOL}	DC Open Loop Voltage Gain, GS_X	5000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		1		MHz	
V_{OXI}	Output Voltage Swing GS_X	−2.17		2.17	V	$R_L \geq 10k\Omega$
C_{LXI}	Load Capacitance, GS_X			50	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, PWRO+, PWRO−		75		mV	Relative to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF	
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO−, Single-Ended Connection	−3.06		3.06	V	$R_L \geq 300\Omega$ with zero volt offset
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO−, Balanced Output Connection	−6.12		6.12	V	$R_L \geq 600\Omega$

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.[1] Input amplifier is set for unity gain,[2] inverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended. All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	−0.15	±0.04	+0.15	dBm0	Signal input of 1.064 Vrms μ-law Signal input of 1.068 Vrms A-law T_A = 25°C, V_{BB} = −5V, V_{CC} = +5V
EmW_{TS}	EmW variation with Temperature and supplies	−0.12		+0.12	dB	±5% supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response (Receive gain tolerance)	−0.15	±0.04	+0.15	dBm0	Measure relative to $0TLP_R$. Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz. T_A = 25°C; V_{BB} = −5V, V_{CC} = +5V.
DmW_{TS}	DmW variation with temperature and supplies	−0.08		+0.08	dB	±5% supplies, 0 to 70°C
$0TLP1_X$	Zero Transmission Level Point Transmit Channel (0dBm0) μ-law		+2.76 +1.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBM0) A-law		+2.79 +1.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP1_R$	Zero Transmission Level Point Receive Channel (0dBm0) μ-law		+5.76 +4.00		dBm dBm	Referenced to 600Ω Referenced to 900Ω
$0TLP2_R$	Zero Transmission Level Point Receive Channel (0dBm0) A-law		+5.79 +4.03		dBm dBm	Referenced to 600Ω Referenced to 900Ω

NOTES:

1. 0dBm0 is defined as the zero reference point of the channel for μ law under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms.
2. Unity gain input amplifier, signal input VF_XI-.

GAIN TRACKING

Reference Level = −10dBm0

Symbol	Parameter	2916 Min	2916 Max	2917 Min	2917 Max	Unit	Test Conditions
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law		±0.25 ±0.5 ±1.2			dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law				±0.25 ±0.5 ±1.2	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
$GT3_X$	Transmit Gain Tracking Error White Noise Input; A-law				TBD	dB	CCITT G.712 Method 1
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law		±0.25 ±0.5 ±1.2			dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law				±0.25 ±0.5 ±1.2	dB dB dB	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0
$GT3_R$	Receive Gain Tracking Error White Noise Input; A-law				TBD	dB	CCITT G. 712 Method 1

NOISE

Symbol	Parameter	2916 Min	2916 Typ	2916 Max	2917 Min	2917 Typ	2917 Max	Unit	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted			15				dBrncO	Unity Gain
N_{XP}	Transmit Noise, Psophometrically Weighted						−75	dBm0p	Unity Gain
N_{RC1}	Receive Noise, C-Message Weighted: Quiet Code			11				dBrncO	D_R = 11111111 Measure at PWRO+
N_{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			12				dBrncO	Input to D_R is zero code with sign bit toggle at 1 kHz rate
N_{RP}	Receive Noise, Psophometrically Weighted						−79	dBm0p	D_R = lowest positive decode level
N_{SF}	Single Frequency Noise End to End Measurement			−50			−50	dBm0	CCITT G.712.4.2
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel		−30			−30		dB	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel		−30			−30		dB	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel		−25			−25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel		−25			−25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs			−71			−71	dB	Input = 0dBm0, Unity Gain, 1.02 kHz, D_R = lowest positive decode level, measure at PWRO+
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs			−71			−71	dB	D_R = 0dBm0, 1.02 kHz, measure at D_X

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2 (2916)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (2917)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_X$	Transmit Signal to Distortion, A-Law White Noise Input; CCITT G.712-Method 1 (2917)	TBD				
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2 (2916)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD2_R$	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (2917)	36 30 25			dB dB dB	0 to −30 dBm0 −30 to −40 dBm0 −40 to −45 dBm0
$SD3_R$	Receive Signal To Distortion, A-Law White Noise Input; CCITT G.712-Method 1 (2917)	TBD				
DP_{X1}	Transmit Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP_{R1}	Receive Single Frequency Distortion Products			−46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD_1	Intermodulation Distortion, End to End Measurement			−35	dB	CCITT G.712 (7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			−40	dBm0	CCITT G. 712 (9)
D_{AX}	Transmit Absolute Delay		245		μs	Fixed Data Rate. CLK_X = 2.048 MHz; 0 dBm0, 1.02 kHz input Signal, Unity Gain. Measure at D_X.
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}		170 95 45 105		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz
D_{AR}	Receive Absolute Delay		190		μs	Fixed Data Rate, CLK = 2.048 MHz; Digital Input is DMW codes. Measure at PWRO + .
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}		45 35 85 110		μs μs μs μs	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz

Input amplifier is set for unity gain, inverting.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at VF_XI-
	16.67 Hz			−30	dB	
	50 Hz			−25	dB	
	60 Hz			−23	dB	
	200 Hz	−1.8		−0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.10	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−32	dB	

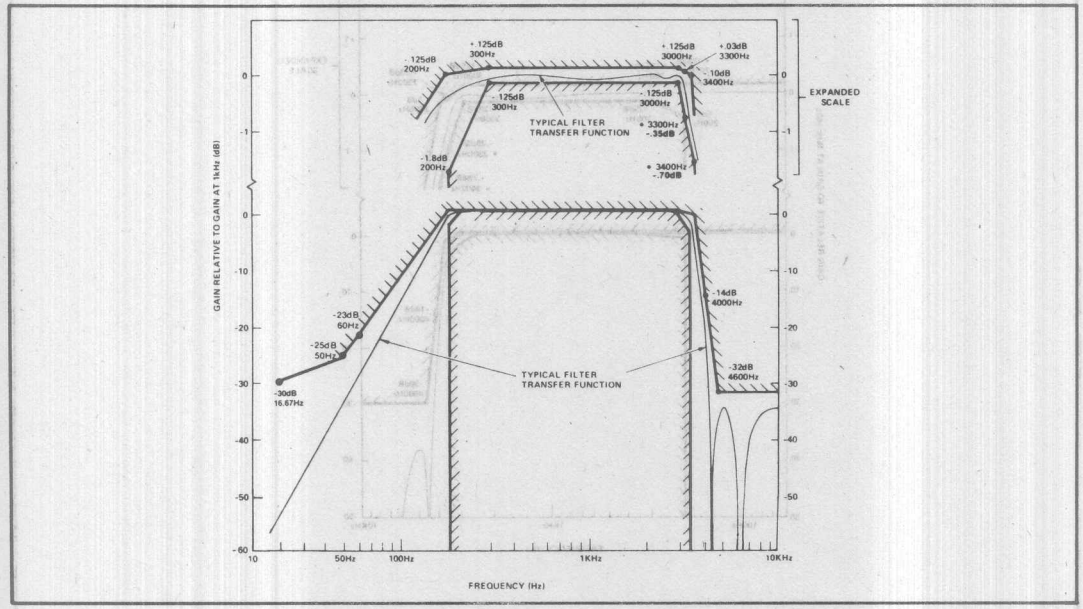


Figure 4. Transmit Channel

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	−0.5		+0.125	dB	
	300 to 3000 Hz	−0.125		+0.125	dB	
	3300 Hz	−0.35		+0.03	dB	
	3400 Hz	−0.7		−0.1	dB	
	4000 Hz			−14	dB	
	4600 Hz and Above			−30	dB	

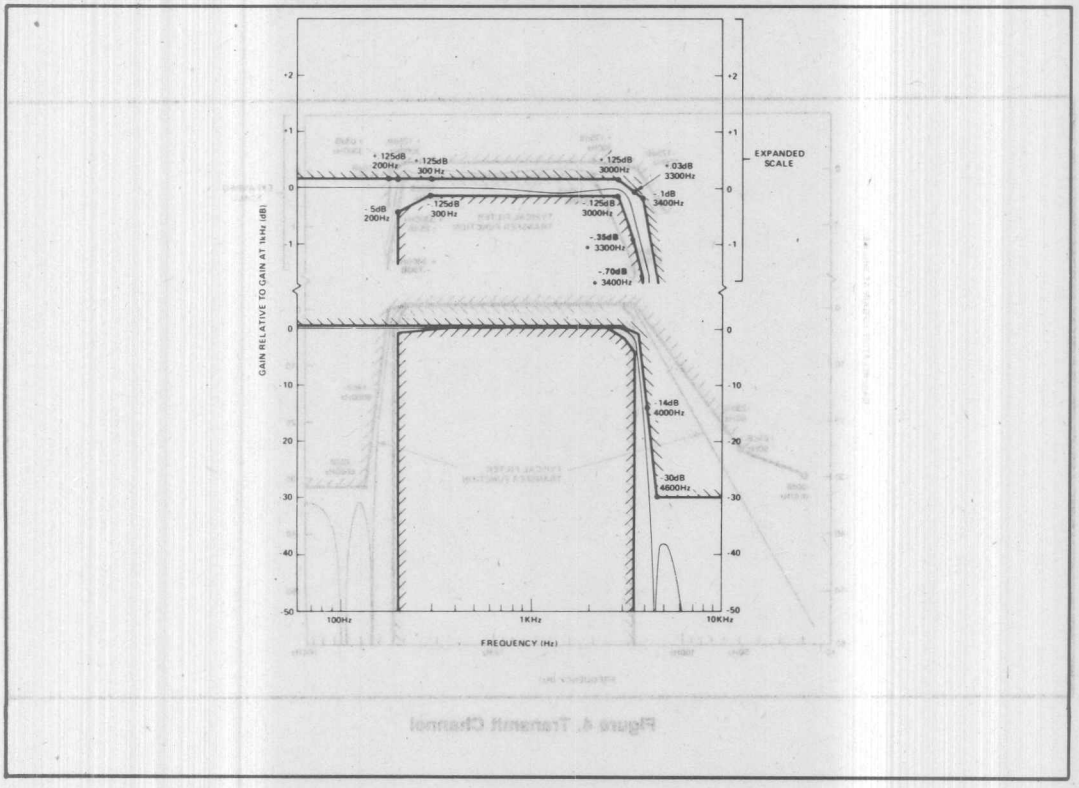


Figure 5. Receive Channel

A.C. CHARACTERISTICS — TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK	488			ns	f_{CLK} = 2.048 MHz
t_{CLK}	Clock Pulse Width	195			ns	CLK
t_{DCLK}	Data Clock Pulse Width	195			ns	64 kHz ≤ f_{DCLK} ≤ 2.048 MHz
t_{CDC}	Clock Duty Cycle	40	50	60	%	CLK
t_r, t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	0 < C_{LOAD} < 100 pf
t_{DDX}	Data Delay from CLK_X	0		145	ns	0 < C_{LOAD} < 100 pf
t_{HZX}	Data Float on TS Exit	60		190	ns	C_{LOAD} = 0
t_{SON}	Timeslot X to Enable	0		145	ns	0 < C_{LOAD} < 100 pf
t_{SOFF}	Timeslot X to Disable	50		190	ns	C_{LOAD} = 0
t_{FSD}	Frame Sync Delay	0		120	ns	

RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	0		120	ns	

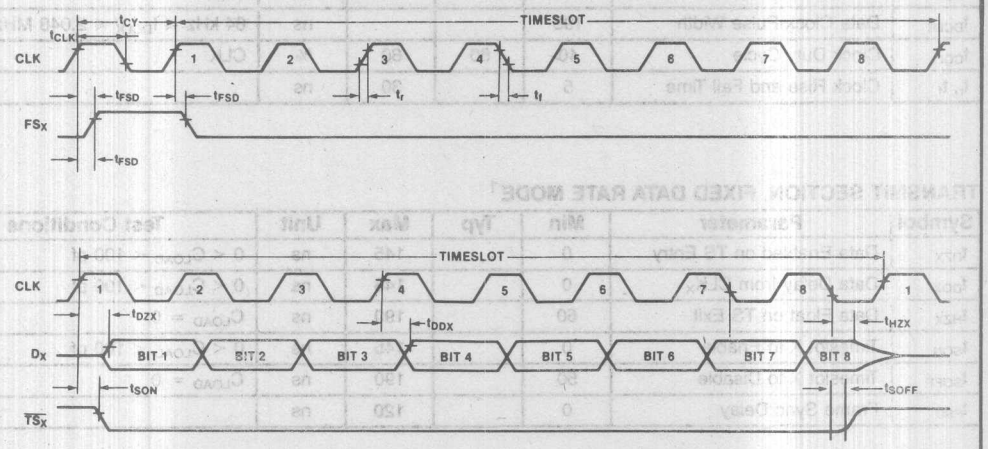
NOTES:

1. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

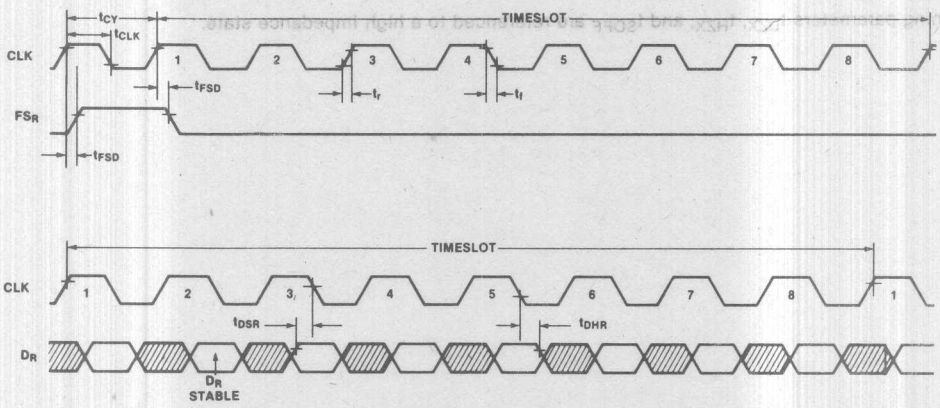
Fixed Data Rate Timing

TRANSMIT TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X$	−80		80	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
f_{DX}	Data Clock Frequency	64		2048	kHz	
t_{DFSX}	Data Delay from FS_x	0		140	ns	t_{TSDX} = 80 ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R$	−80		80	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
f_{DR}	Data Clock Frequency	64		2048	kHz	
t_{SER}	Timeslot End Receive Time	0			ns	

64 KB OPERATION, VARIABLE DATA RATE MODE

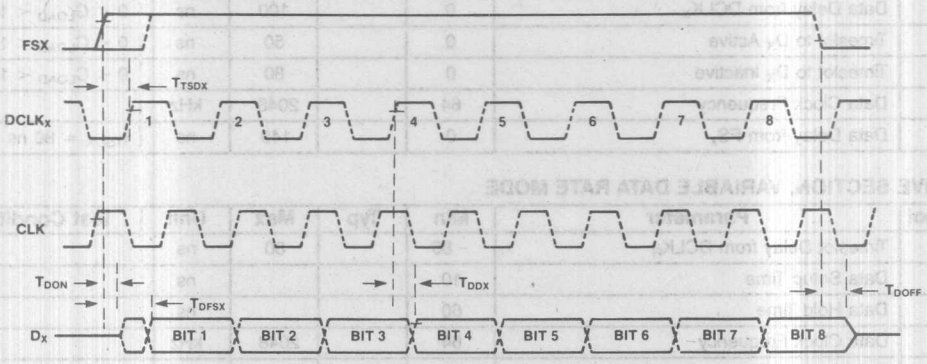
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	µs	

NOTES:

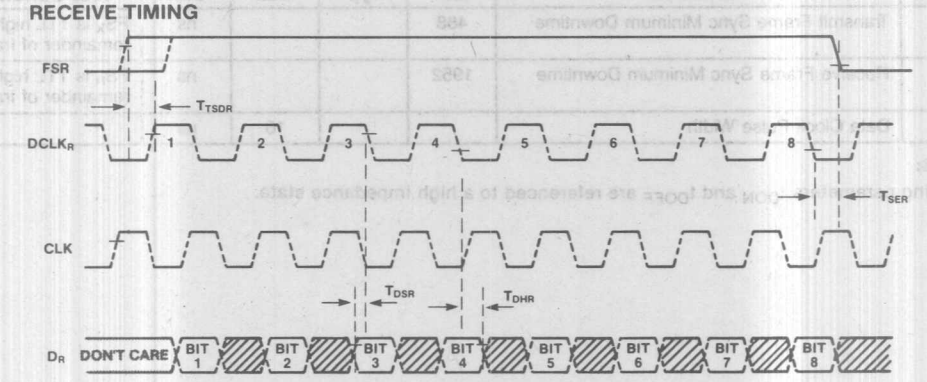
1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.

VARIABLE DATA RATE TIMING

TRANSMIT TIMING



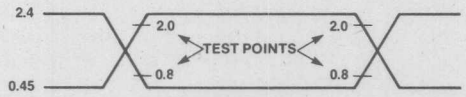
RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DON} AND t_{OFF} WHICH REFERENCE A HIGH IMPEDANCE STATE

A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" and 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

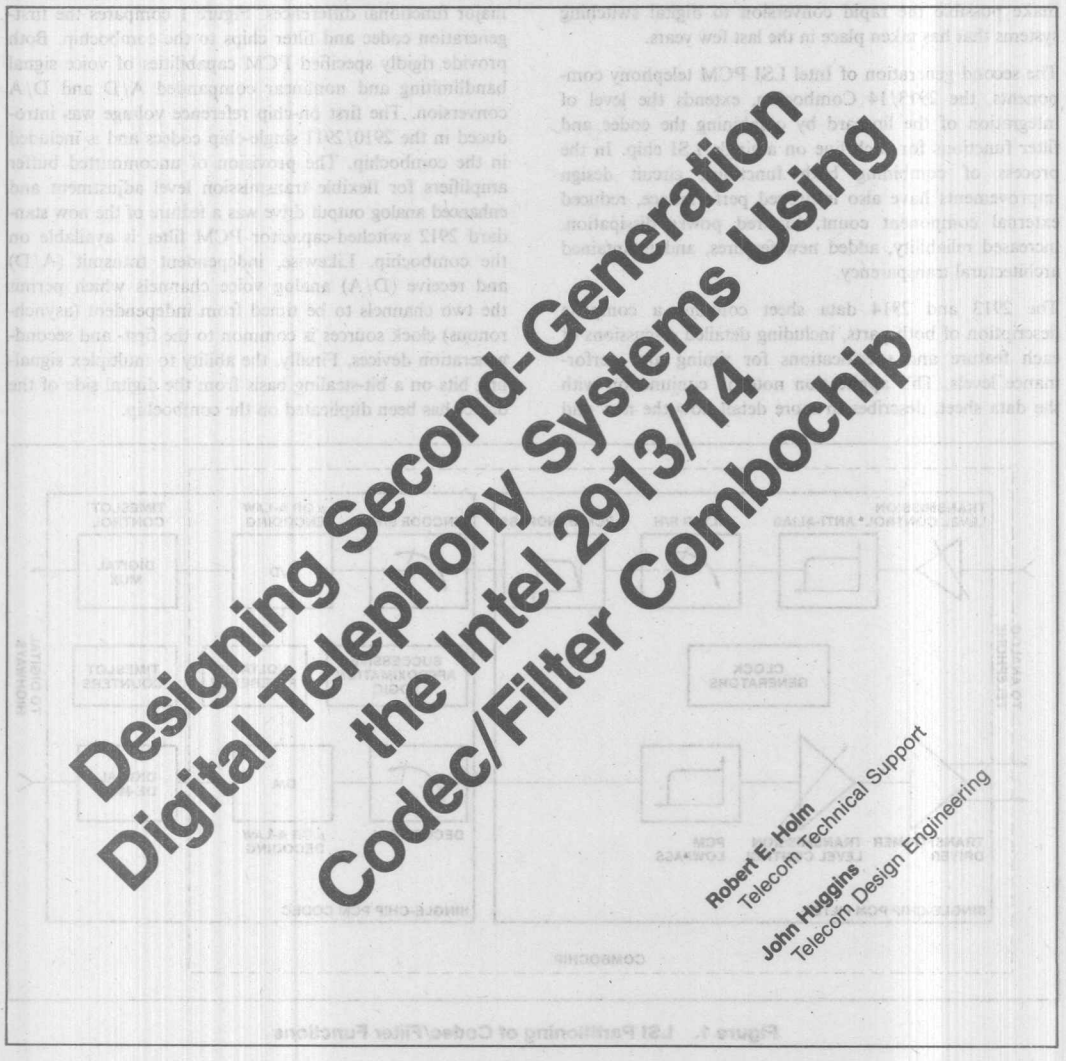
intel

APPLICATION NOTE

AP-142

February 1982

Designing Second-Generation Digital Telephony Systems Using the Intel 2913/14 Codec/Filter Combochip



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1.0 INTRODUCTION

This application note describes the features and capabilities of the 2913 and 2914 codec/filter combochips, and relates these capabilities to the design and manufacturing of transmission and switching linecards.

1.1 Background

The first generation of per line codecs (Intel 2910A/11A) and filters (Intel 2912A) economically integrated the analog-digital conversion circuits and PCM formatting circuits into one chip and the filtering and gain setting circuits into another chip. These two chips helped to make possible the rapid conversion to digital switching systems that has taken place in the last few years.

The second generation of Intel LSI PCM telephony components, the 2913/14 Combochip, extends the level of integration of the linecard by combining the codec and filter functions for each line on a single LSI chip. In the process of combining both functions, circuit design improvements have also improved performance, reduced external component count, lowered power dissipation, increased reliability, added new features, and maintained architectural transparency.

The 2913 and 2914 data sheet contains a complete description of both parts, including detailed discussions of each feature and specifications for timing and performance levels. This application note, in conjunction with the data sheet, describes in more detail how the new and improved features help in the design of second-generation linecards first by comparing the two generations of components to see where the improvements have been made, and then by discussing specific design considerations.

1.2 Comparison of First- and Second-Generation Component Capabilities

The combochip represents a higher level of component integration than the devices it replaces and, because of the economics of LSI (replacing two chips with one), ultimately will cost significantly less at the component level. But comparison of the combochip block diagram with first-generation single-chip codec and filter reveals few major functional differences. Figure 1 compares the first-generation codec and filter chips to the combochip. Both provide rigidly specified PCM capabilities of voice signal bandlimiting and nonlinear companded A/D and D/A conversion. The first on-chip reference voltage was introduced in the 2910/2911 single-chip codecs and is included in the combochip. The provision of uncommitted buffer amplifiers for flexible transmission level adjustment and enhanced analog output drive was a feature of the now standard 2912 switched-capacitor PCM filter is available on the combochip. Likewise, independent transmit (A/D) and receive (D/A) analog voice channels which permit the two channels to be timed from independent (asynchronous) clock sources is common to the first- and second-generation devices. Finally, the ability to multiplex signalling bits on a bit-stealing basis from the digital side of the device has been duplicated on the combochip.

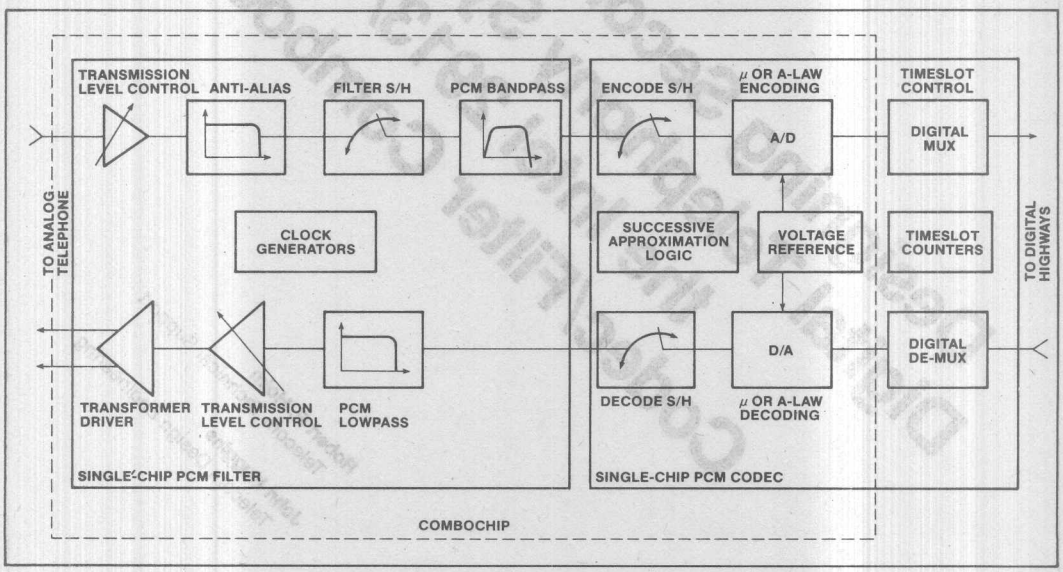


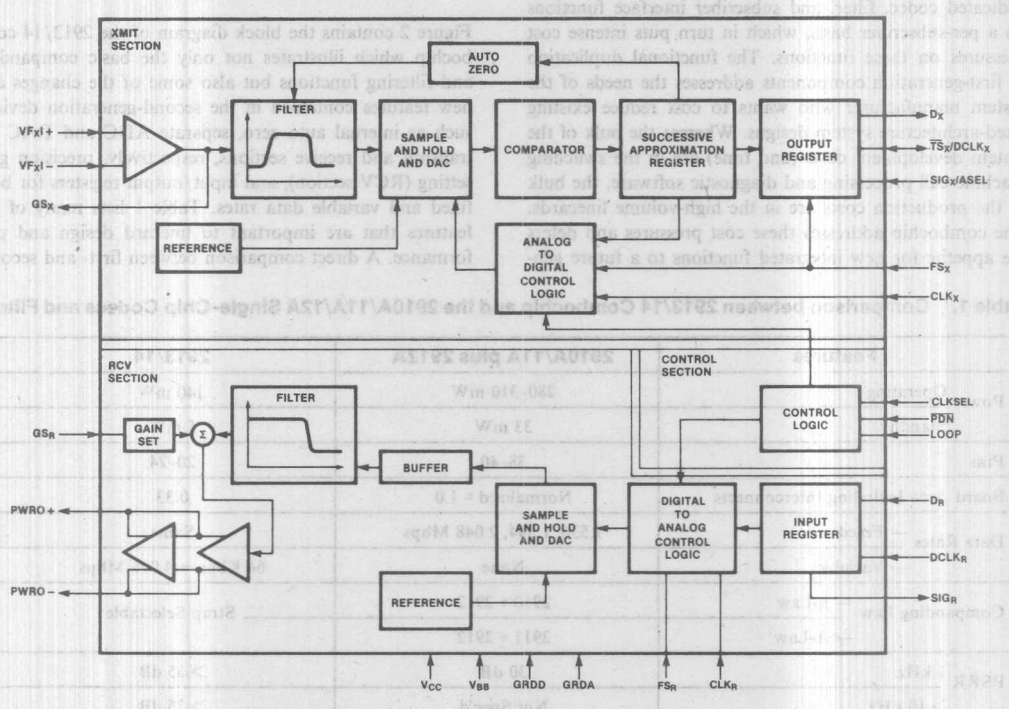
Figure 1. LSI Partitioning of Codec/Filter Functions

Data traffic-conscious systems manufacturers now provide dedicated codec, filter, and subscriber interface functions on a per-subscriber basis, which in turn puts intense cost pressures on these functions. The functional duplication of first-generation components addresses the needs of the system manufacturer who wants to cost reduce existing fixed-architecture system designs. Whereas the bulk of the system development costs (and time) are in the switching machine call processing and diagnostic software, the bulk of the production costs are in the high-volume linecards. The combochip addresses these cost pressures and defers the appetite for new integrated functions to a future generation of PCM components.

Figure 2 contains the block diagram of the 2913/14 combochip which illustrates not only the basic companding and filtering functions but also some of the changes and new features contained in the second-generation devices, such as internal auto zero, separate ADC and DAC for transmit and receive sections, respectively, precision gain setting (RCV section), and input/output registers for both fixed and variable data rates. Table 1 lists many of the features that are important to linecard design and performance. A direct comparison between first- and second-

Table 1. Comparison between 2913/14 Combochip and the 2910A/11A/12A Single-Chip Codecs and Filters

Features	2910A/11A plus 2912A	2913/14
Power — Operating	280–310 mW	140 mW
Power — Standby	33 mW	5 mW
Pins	38–40	20–24
Board Area Including Interconnects	Normalized = 1.0	0.33
Data Rates — Fixed	1.536, 1.544, 2.048 Mbps	Same
Data Rates — Variable	None	64 Kbps → 4.096 Mbps
Companding Law — μ-Law	2910 + 2912	Strap Selectable
Companding Law — A-Law	2911 + 2912	
PSRR 1 kHz	30 dB	> 35 dB
PSRR > 10 kHz	Not Spec'd	> 35 dB
Gain Setting	Trim Using Pot Necessary	Precision Resistors Eliminate Trim Req.
Operating Modes — Direct	yes	yes
Operating Modes — Timeslot Assign	yes	no
On-Chip Vref	yes	yes
ICN — half channel improvement	15 dBrncO Transmit 11 dBrncO Receive	15 dBrncO Transmit 11 dBrncO Receive
S/D — half channel improvement	See Data Sheet	See Section 2.0
GT — half channel improvement	See Data Sheet	See Section 2.0
Power Down (Standby)	PDN Pin	Frame Sync Removal or PDN Pin
Signalling	2910-8th Bit	2914-8th Bit
Auto Zero	External	Internal
S & H Caps	External Transmit Internal Receive	Internal
Test Modes	None	Design Tests Manufacturing Test On-Line Operational Tests
Encoder Implementation	Resistive Ladder	Capacitive Charge Redistribution Ladder
Filter/Gain Trim	Fuse Blowing ±0.2 dB	Fuse Blowing ±0.04 dB



(a) Combochip Block Diagram

V_{BB}	Power (–5V)	GS_X	Transmit Gain Control
PWRO+, PWRO–	Power Amplifier Outputs	$VF_XI–$, VF_XI+	Analog Inputs
GS_R	Receive Gain Control	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG_X	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-law Select
SIG_R	Receive Signaling Bit Output	$\overline{TS}_X$	Timeslot Strobe/Buffer Enable
$DCLK_R$	Receive Variable Data Clock	$DCLK_X$	Transmit Variable Data Clock
D_R	Receive PCM Input	D_X	Transmit PCM Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

(b) Combochip Pin Names

Figure 2. Block Diagram of 2913/14 Combochip

generation products shows the significant improvement in the combochip both in performance levels and system flexibility.

2.0 DESIGN CONSIDERATIONS

The key point with the 2913/14 is that it will result in a linecard that performs better and costs less than any two-chip codec/filter solution. The lower cost results from many factors, as seen in Table 2. Both direct replacement costs and less tangible design and manufacturing time savings combine to yield lower recurring and nonrecurring costs. As an example, the wider margins to transmission specs and the higher power supply rejection ratios of the 2913/14 will both shorten the design time needed to build and test the linecard prototype and reduce the reject rate on the manufacturing line.

Table 2. 2913/14 Factors which Lower the Cost of Linecard Design and Manufacturing

- Lower LSI Cost (2914 vs. 2910/11 + 2912)
- Fewer External Components
- Less Board Area
- Shorter Design/Prototype Cycle
- Better Yields/Higher Reliability
- Lower Power/Higher Density

Part of the recurring cost of linecard production is the efficiency of the manufacturing line in turning out each board. This is measured in both parts cost and time. Average manufacturing time is strongly effected by the line yield, i.e., the reject rate reliability. A linecard using the 2913/14 has many labor-saving features, which also increases the *reliability* of the manufacturing process. Some of these features are detailed in Table 3.

The combination of fewer parameters to trim (gain, reference voltage, etc.), tolerance to wider power supply variations, and on-chip test modes make the linecard very manufacturable compared to first-generation designs.

Probably the most obvious improvement in linecard design based around the 2913/14 is the reduction in linecard PCB area needed compared to two-chip designs. The combination of the codec and filter into a single package alone reduced the LSI area by one-third. Table 4 shows many of the other ways in which board area is conserved. In general, it reduces to fewer components, more on-chip features, and layout of the chip resulting in an efficient board layout which neatly separates the analog and digital signals both inside the chip and on the board.

Table 3. 2914 Factors which Increase Linecard Manufacturing Yields and Efficiency

- Higher Reliability
 - —Fewer connections & components
 - —more integrated packaging
 - —more margin to specs
 - —lower power
 - —NMOS proven process
 - —Less sensitive to parameter variations
- Fewer Manufacturing Steps
 - —no gain trimming
 - —on chip Vref
 - —wide power supply tolerance
 - —on chip test modes
 - —wide margins to specs

Table 4. Design Factors for 2914 which Reduce Linecard PCB Area

- Integrated Packaging
 - —2914 vs. 2910/11 + 2912 = 1/3 board area
 - —2913 takes even less space
- Fewer Interconnects/Components
 - —codec/filter combined
 - —on-chip reference voltage
 - —on-chip auto zero
 - —on-chip capacitors
 - —no gain trim components
 - —no voltage regulators
- Efficient Layout (Facilitates Auto Insertion,
 - —analog/digital sections separated on chip
 - —digital traces can cross under chip
 - —two power supplies only
 - —low power/high density

Table 5. 2913/14 Operating Mode Options Add Flexibility to Linecard Design

Option	Mode Control Pins	Results of Mode Selection	
		2914 (24 pin)	2913 (20 pin)
Companding Law	SIGX/ASEL	A-Law or μ-Law + Signalling	A-Law/μ-Law, no Signalling
Power Down	$\overline{PDN}$	Transmit & Receive Side Go To Standby Power (5 mW)	
	FS_X & FS_R Removed	Same (12 mW)	
	FS_X Removed	Transmit Side Goes to Standby (110 mW)	
	FS_R Removed	Receive Side Goes to Standby (70 mW)	
Data Rate	$= V_{CC}/GRDD/V_{BB}$ $DCLK_R = V_{BB}$	1.536/1.544/2.048 Mbps in fixed data rate mode	
	$= V_{CC}/GRDD/V_{BB}$ $DCLK_R$ = Clock	Variable Data Rate Mode from 64 Kbps to 4.096 Mbps, No Signalling	
Test Modes	LOOP = V_{CC}	Implements Analog Loopback	No Loopback Capability
	$\overline{PDN} = V_{BB}$	Provides Access to Transmit Codec Through ASEL and $\overline{TSX}$ Pins	
	$D_R = V_{BB}$	Provides Access to RCV Filter Input at $DCLK_R$ and Transmit Filter Outputs at ASEL and $\overline{TSX}$ Pins	

Many of the factors discussed above—which result in efficient, cost-effective linecard designs—are discussed in more detail both in the 2913/14 data sheet and in the following sections of this note.

2.1 Operating and Test Mode Selection

A key to designing with the 2913/14 combo is the wide range of options available in configuring, either with strap options or in real time, the different modes of operation. The 2913 combochip (20 pins) is specifically aimed at synchronous switching systems (remote concentrators, PABXs, central offices) where small package size is especially desirable. The 2914 combochip (24 pins) has additional features which are most suitable for applications requiring 8th-bit signalling, asynchronous operation, and remote testing of transmission paths (e.g., channel banks). Once the specific device is selected, there is a wide range of operating modes to use in the card design, as seen in Table 5. This table lists the optional parameters and the pins which control the operating mode. The result of selecting a mode is listed for both the 2913 and 2914.

The purpose of offering these options is to ensure that the 2913/14 combo will accommodate any existing linecard design with architectural transparency. At the same time, features were designed in to facilitate design and manufacturing testing to reduce overall cost of development and production.

2.2 Data Rate Modes

Any rapid conversion scenario presumes that the combochip will fit existing system architectures (retrofit) without significant system timing, control, or software modifications. To this end, two distinct user-selectable timing modes are possible with the combochip. For purposes of discussion, these are designated (a) fixed data rate timing (FDRT) and (b) variable data rate timing (VDRT).

FDRT is identical to the 2910/2911 codec timing in which a single high-speed clock serves both as master clock for the codec/filter internal conversion/filtering functions and as PCM bit clock for the high-speed serial PCM data bus over which the combochip transmits and receives its digitized voice code words. In this mode, PCM bit rates are necessarily confined to one of three distinct frequencies (1.536 MHz, 1.544 MHz, or 2.048 MHz). Many recently designed systems employ this type of timing which is sometimes referred to as burst-mode timing because of the low duty cycle of each timeslot (i.e., channel) on the time division multiplexed PCM bus. It is possible for up to 32 active combochips to share the same serial PCM bus with FDRT.

VDRT (sometimes referred to as shift register timing), by comparison, utilizes one high-speed master clock for the combochip internal conversion/filtering functions and a separate, variable frequency, clock as the PCM bit clock for the serial PCM data bus. Because the serial PCM data rate is independent of internal conversion timing, there is considerable flexibility in the choice of PCM data rate. In this mode the master clock is permitted to be 1.536 MHz, 1.544 MHz, or 2.048 MHz, while the bit clock can be any rate between 64 kHz and 4.096 MHz. In this mode it is possible to have a dedicated serial bus for each combochip or to share a single serial PCM bus among as many as 64 active combochips.

Thus, the two predominant timing configurations of pres-

ent system architectures are served by the same device, allowing, in many cases, linecard redesign without modification of any common system hardware or software. Additional details relating to the design of systems using either mode are found in section 3.0.

2.3 Margin to Performance Specifications

The combochip benefits from design, manufacturing, and test experience with first-generation PCM products on the part of the system manufacturer, component suppliers, and test equipment suppliers. The sub-millivolt PCM measurement levels and tens of microvolts accuracy requirements on the lowest signal measurements often result in tester correlation problems, yield losses, and excess costs for system and PCM component manufacturers alike. Thus additional performance margin built into the PCM components themselves will have its effect on line circuit costs even though the system transmission specifications may not reflect the improved performance margin.

Half channel measurements have been made of the transmission parameters—gain tracking (GT), signal to distortion ratio (S/D), and idle channel noise (ICN).

Gain Tracking—Figure 3 shows the gain tracking data for both the transmit and receive sides of the combo using both sine wave testing (CCITT G712.11 Method 2) and white noise testing (CCITT G712.11 Method 1). The data shows a performance very nearly equal to the theoretically best achievable using both test techniques. End to end measurements, although not spec'd, also show a corresponding good performance with errors less than or equal to the sum of the half channel values.

Signal to Distortion Ratio—This is a measure of the system linearity and the accuracy in implementing the companding codes. Figure 4 shows the excellent perfor-

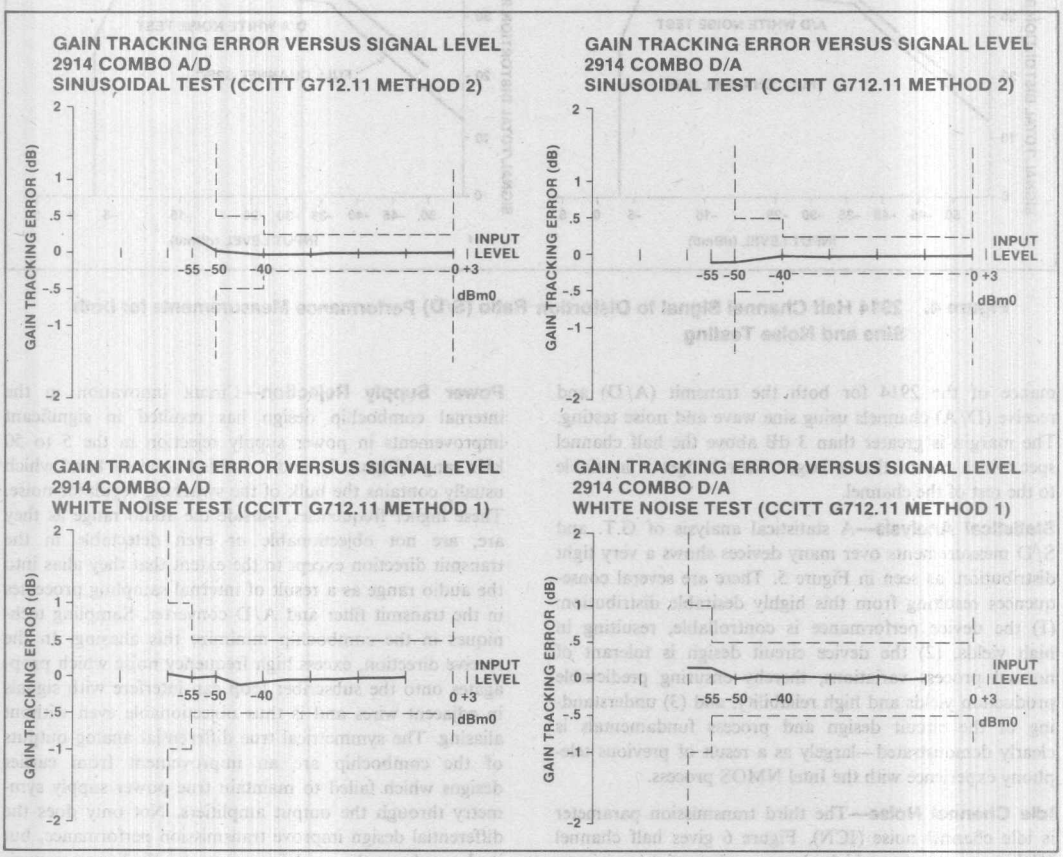


Figure 3. 2914 Half Channel Gain Tracking Performance Measurements for both Sine and Noise Testing

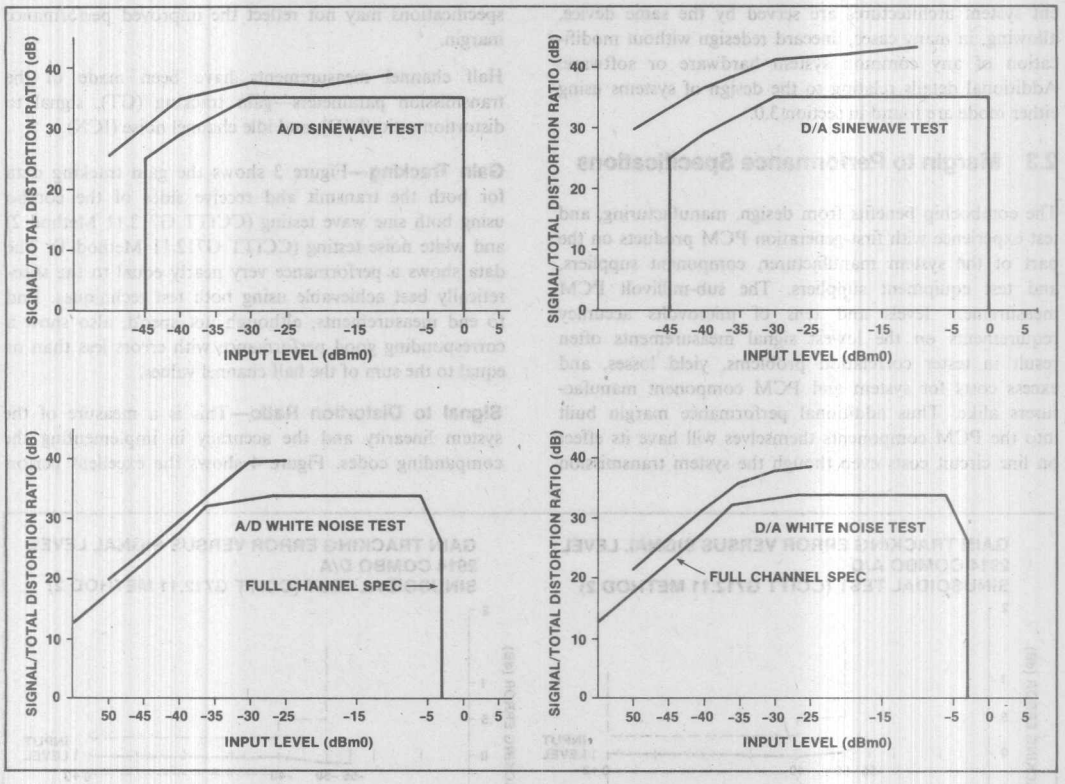


Figure 4. 2914 Half Channel Signal to Distortion Ratio (S/D) Performance Measurements for both Sine and Noise Testing

mance of the 2914 for both the transmit (A/D) and receive (D/A) channels using sine wave and noise testing. The margin is greater than 3 dB above the half channel spec which means that a larger error budget is available to the rest of the channel.

Statistical Analysis—A statistical analysis of G.T. and S/D measurements over many devices shows a very tight distribution, as seen in Figure 5. There are several consequences resulting from this highly desirable distribution: (1) the device performance is controllable, resulting in high yields, (2) the device circuit design is tolerant of normal process variations, thereby ensuring predictable production yields and high reliability, and (3) understanding of the circuit design and process fundamentals is clearly demonstrated—largely as a result of previous telephony experience with the Intel NMOS process.

Idle Channel Noise—The third transmission parameter is idle channel noise (ICN). Figure 6 gives half channel ICN measurements which show a substantial margin to specification.

Power Supply Rejection—Circuit innovation in the internal combochip design has resulted in significant improvements in power supply rejection in the 5 to 50 kHz range (Figure 7), and it is this frequency band which usually contains the bulk of the switching regulator noise. These higher frequencies, outside the audio range as they are, are not objectionable or even detectable in the transmit direction except to the extent that they alias into the audio range as a result of internal sampling processes in the transmit filter and A/D converter. Sampling techniques in the combochip minimize this aliasing. In the receive direction, excess high frequency noise which propagates onto the subscriber loop can interfere with signals in adjacent wires and is thus objectionable even without aliasing. The symmetrical true differential analog outputs of the combochip are an improvement from earlier designs which failed to maintain true power supply symmetry through the output amplifiers. Not only does the differential design improve transmission performance, but it also reduces the need for power supply bypass capacitors, thereby saving component cost on the linecard.

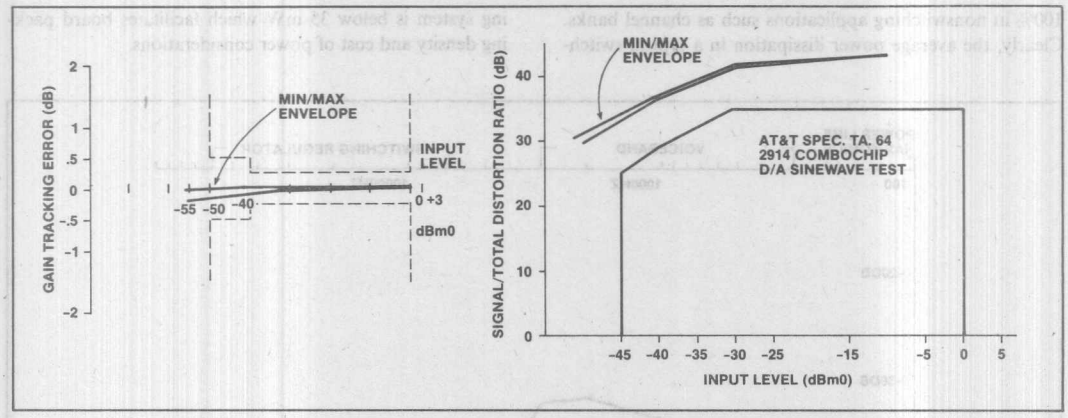


Figure 5. Statistical Analysis of Transmission Performance Showing Tight Distribution over many Devices

	WEIGHTING	ICN
A/D	C MESSAGE	15 dBrnCO
D/A	C MESSAGE	11 dBrnCO

Figure 6. 2914 Idle Channel Noise (ICN) Measurements

Autozero—The autozero circuit is contained completely on-chip. It automatically centers the signal/noise distribution at the encoder input. This ensures minimal ICN due to bit toggeling and also maintains maximum sensitivity to the AC signals of interest.

2.4 Power Conservation

Figure 8 illustrates typical power consumption and office equipment dissipation for a resistive line biasing arrangement (with no loop current limiting) and for the per-line PCM components. It can be seen that overall line circuit power consumption and dissipation are strong functions of subscriber loop resistance, and are dominated by line biasing current regardless of loop length. It can also be seen that the combochip achieves significant reductions in PCM component contributions relative to both the 2910A/2912A and 2910/2912. Present residential traffic characteristics are such that the PCM components are active less than 10% of the time, and in its low-power standby state, the combochip power dissipation drops to typically 5 mW as the line current (and dissipation) goes to its background on-hook leakage level of typically a few milliwatts (but for very leaky lines, as much as 50–500 mW).

The concern for linecard power consumption and dissipation is related both to the cost of providing power and to the system density problem involving convection heat removal from the linecards. Consequently, much recent line circuit development activity centers on elimination of the inefficient resistive line current feed both by current limiting in short loops and by more exotic and expensive per-line dc-dc converters. For both present-generation designs and cost-reduction redesigns, the typical combochip dissipation of 140 mW active/5 mW standby will allow system board packing density improvements and power supply cost reductions.

A closer look at the effect of loading (duty cycle) on the average power dissipation of a combochip is given in Table 6. Typical loading percents run as low as 5% for very large switching systems (thousands of lines) up to

Table 6. Typical Power Dissipation Per Line Using 2914 Combochip

	Duty Cycle	Power Dissipation
Central Office	5%	12 mW
PABX	15%	25 mW
Peak Hour C.O.	50%	73 mW
Channel Bank	100%	140 mW

100% in nonswitching applications such as channel banks. Clearly, the average power dissipation in a typical switching system is below 35 mW which facilitates board packing density and cost of power considerations.

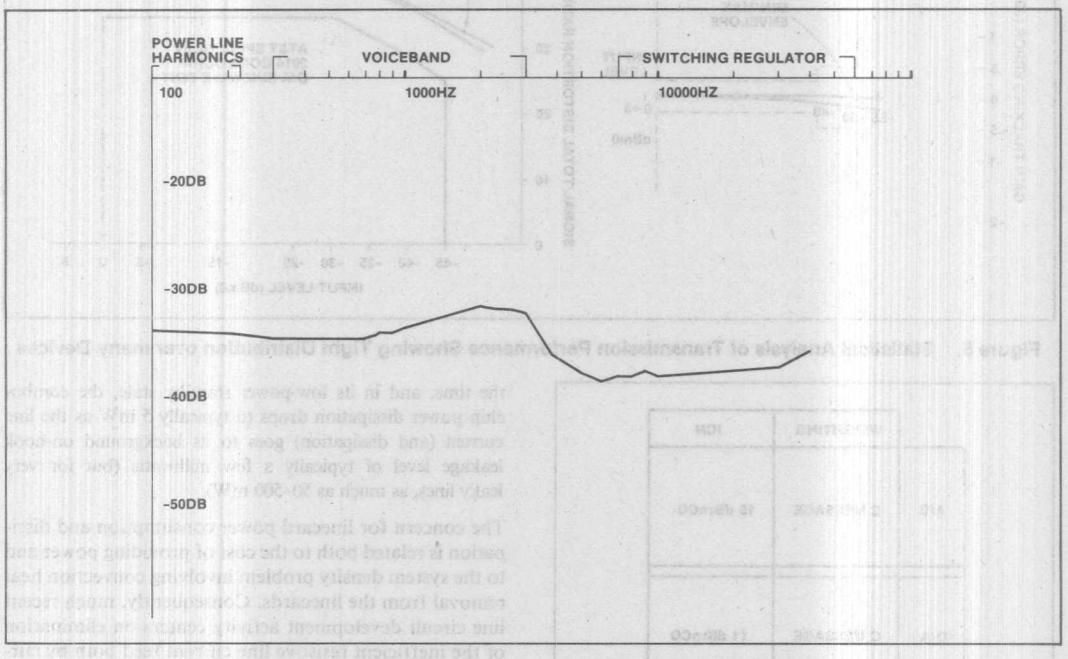


Figure 7. Wideband 2914 Power Supply Rejection Ratio (PSRR)

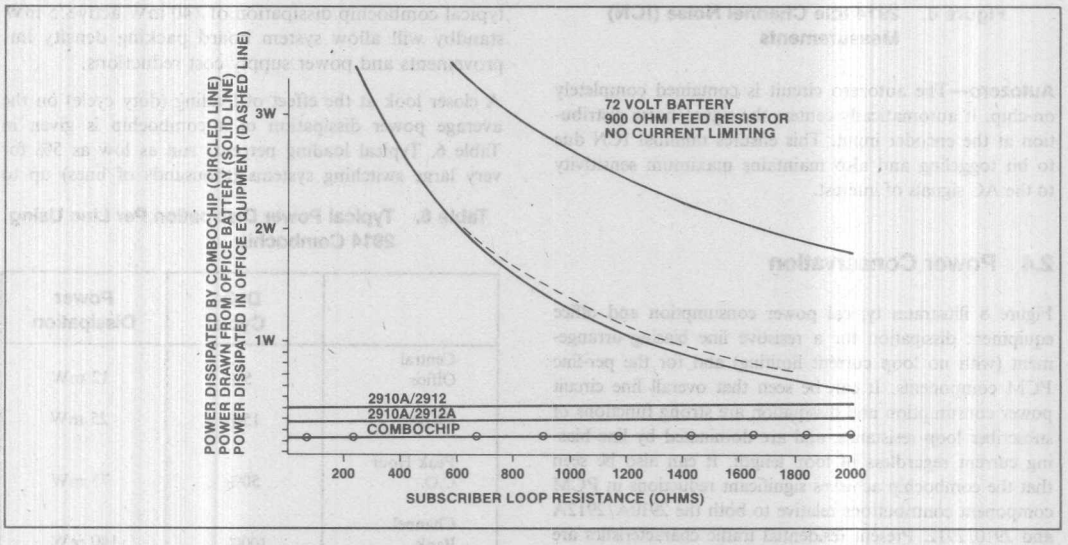


Figure 8. Line Circuit Power Consumption and Dissipation Curves

2.5 Elimination of Gain Trim in the Line Circuit

Four resistors—R1-R4 of Figure 9—on the transformer side of the PCM components are used to establish appropriate transmission levels at the PCM components and are, at first glance, equivalent in the two cases. However, a significant reduction in linecard manufacturing costs associated with individual line trim (or mop-up) is possible with the combochip. The need for this trim is dictated by system gain contrast specifications which typically require that the line-to-line gain variation shall not exceed 0.5 dB, which translates to 0.25 dB for each (transmit and receive) channel. Table 7 shows that the major portion of this gain variation has previously been in the nominal insertion loss of the PCM filter and in the uncertainty of the reference voltage of the codec. With this cumulative 0.15 dB uncertainty in the PCM components themselves, the system manufacturer had no choice but to resort to the cost and manufacturing complexity of the active trim. The combochip, however, can be trimmed during its manufacture to a nominal tolerance of ±0.04 dB which includes uncertainties in both the filter and codec voltage reference functions. This leaves 0.21 dB uncertainty to variations in the other line circuit elements and to temperature and supply variations.

The variation in combochip gain with supply and temperature has also been improved to allow as low as

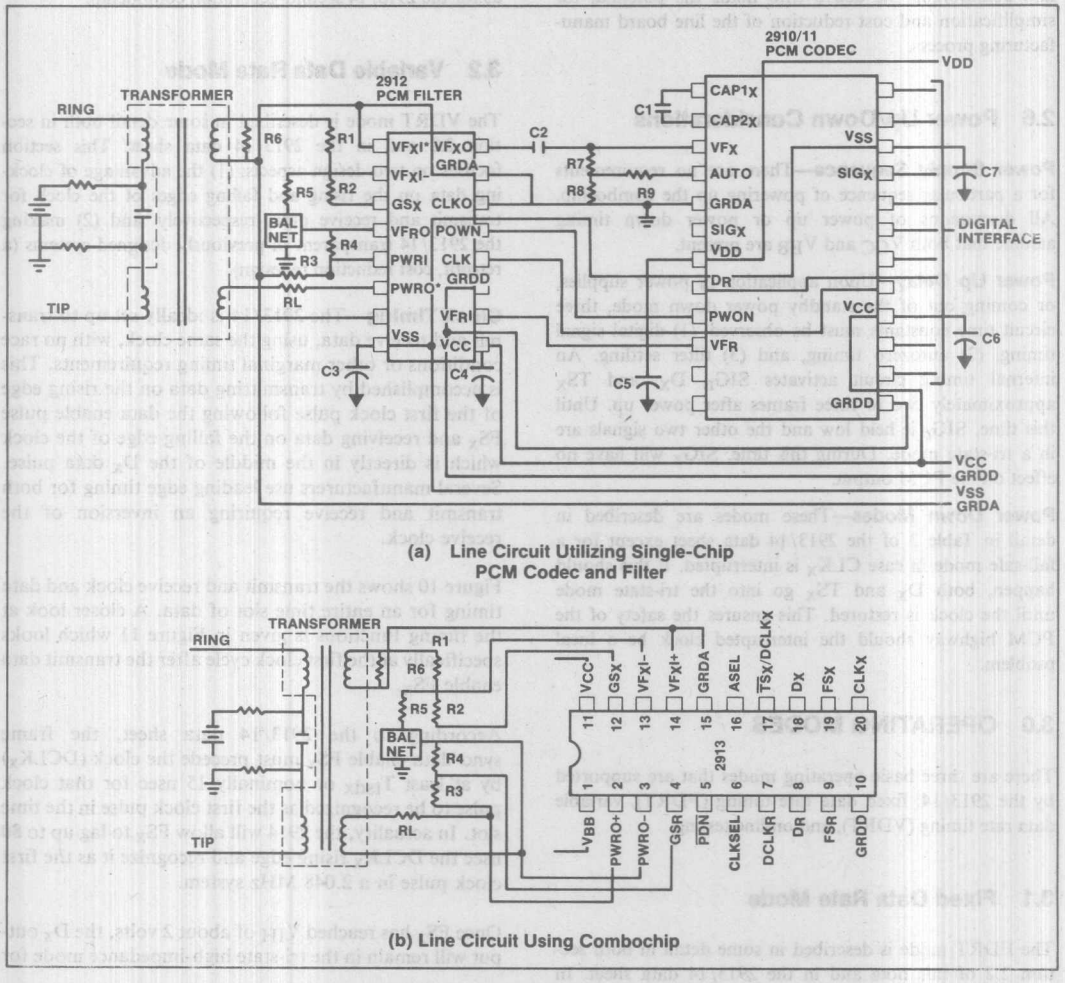


Figure 9. Schematics of the Codec/Filter Function and the 2/4 Wire Hybrid Transformers

Table 7. Gain Trim Budget for Codec/Filter Functions

Device	Manufacturing Uncertainty (Initial)	ΔT ΔSupplies	Total	Variation* Budget for Other Components
2910	±0.1	±0.1		
2912	±0.05	±0.05		
	±0.15	±0.15	±0.3 dB	0 dB
2914	±0.04	±0.08	±0.12 dB	±0.13 dB

*Assumes 0.5 dB end to end gain contrast specification.

0.08 dB variation over supplies and temperature so that more than half the system specification could be reserved for transformer, wiring, and resistor uncertainties. This possibility of using fixed precision gain trim components and abandoning the active trim holds the potential for simplification and cost reduction of the line board manufacturing process.

2.6 Power Up/Down Considerations

Power Supply Sequence—There are no requirements for a particular sequence of powering up the combochip. All discussions of power up or power down timing assume that both V_{CC} and V_{BB} are present.

Power Up Delay—Upon application of power supplies, or coming out of the standby power down mode, three circuit time constants must be observed: (1) digital signal timing, (2) autozero timing, and (3) filter settling. An internal timing circuit activates SIG_r, D_X, and TS_X approximately two to three frames after power up. Until this time, SIG_r is held low and the other two signals are in a tri-state mode. During this time, SIG_X will have no effect on the PCM output.

Power Down Modes—These modes are described in detail in Table 3 of the 2913/14 data sheet except for a fail-safe mode in case CLK_X is interrupted. If this should happen, both D_X and TS_X go into the tri-state mode until the clock is restored. This ensures the safety of the PCM highway should the interrupted clock be a local problem.

3.0 OPERATING MODES

There are three basic operating modes that are supported by the 2913/14: fixed data rate timing (FDRT), variable data rate timing (VDRT), and on-line testing.

3.1 Fixed Data Rate Mode

The FDRT mode is described in some detail in both section 2.2 of this note and in the 2913/14 data sheet. In addition, Intel Application Note AP-64 (Data Conversion, Switching, and Transmission using the Intel 2910A/2911A codec and 2912 PCM filter) also describes the basics of using the fixed data rate mode for first-generation codecs and filters which is essentially the same as for the 2913/14 second-generation combochip.

3.2 Variable Data Rate Mode

The VDRT mode is described in some detail both in section 2.2 and in the 2913/14 data sheet. This section focuses on two design aspects: (1) the advantage of clocking data on the rising and falling edges of the clock for transmit and receive data, respectively, and (2) making the 2913/14 transparent in previously designed systems (a retrofit, cost reduction redesign).

Clock Timing—The 2913/14 is ideally set up to transmit and receive data, using the same clock, with no race conditions or other marginal timing requirements. This is accomplished by transmitting data on the rising edge of the first clock pulse following the data enable pulse FS_X and receiving data on the falling edge of the clock which is directly in the middle of the D_X data pulse. Several manufacturers use leading edge timing for both transmit and receive requiring an inversion of the receive clock.

Figure 10 shows the transmit and receive clock and data timing for an entire time slot of data. A closer look at the timing functions is given in Figure 11 which looks specifically at the first clock cycle after the transmit data enable FS_X.

According to the 2913/14 data sheet, the frame sync/data enable FS_X must precede the clock ($DCLK_X$) by at least T_{tsdx} or nominally 15 nsec for that clock pulse to be recognized as the first clock pulse in the time slot. In actuality, the 2914 will allow FS_X to lag up to 80 nsec the $DCLK_X$ rising edge and recognize it as the first clock pulse in a 2.048 MHz system.

Once FS_X has reached V_{IH} of about 2 volts, the D_X output will remain in the tri-state high-impedance mode for

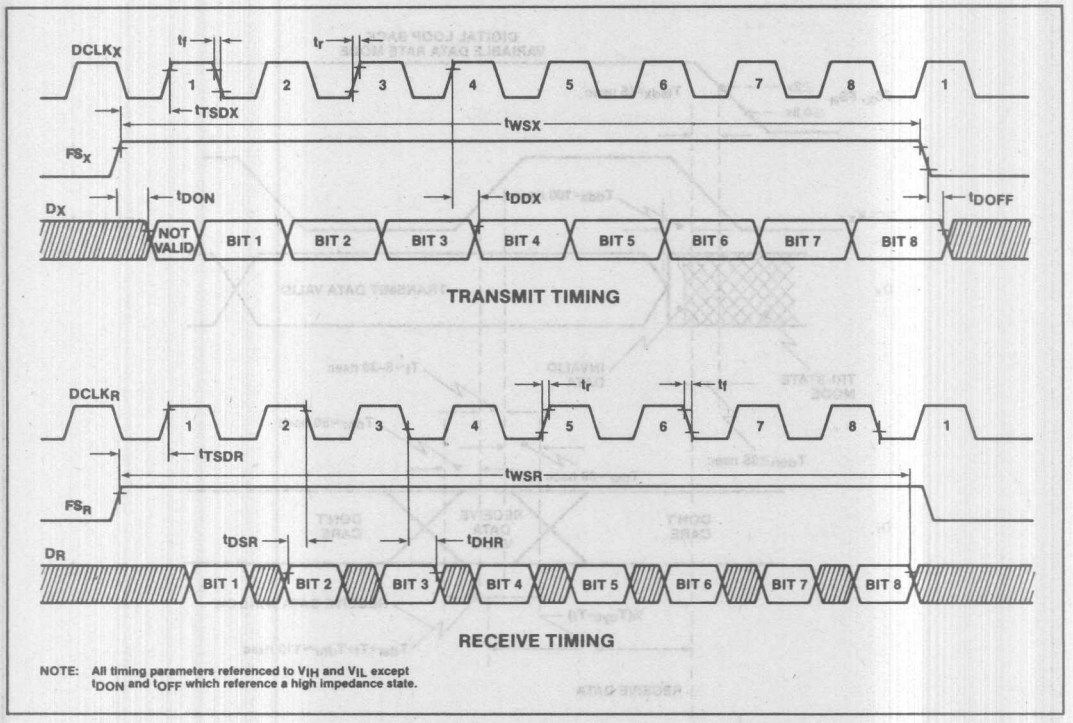


Figure 10. Variable Data Rate Timing for an Entire Time Slot

T_{don} or about 35 nsec longer. It then comes out of tri-state and will represent some data which is invalid until the valid data is available T_{DDX} or about 75 nsec (100 nsec worst case) after the clock rising edge. This means there is about 90 nsec of invalid data after the tri-state mode. At this point there is valid data on the D_X highway that lasts for approximately one full clock cycle.

Since the D_X highway is tied directly to the D_r highway in digital loopback, the valid data above is now available to the receive channel with some propagation delay. The receiver is only interested in the data for about a 50 nsec (110 nsec worst case) window centered about the falling edge of the $DCLK_r$ clock which occurs about half a clock cycle from the FS_r rising edge. The window width is equal to the data set-up time. T_{dsr}, plus the clock fall time, T_f, plus the data hold time, T_{dhr}. Information at any other time on the D_r highway falls into the DON'T CARE category.

Retrofitting the 2913/14—Several switching/transmission systems have been designed using first-generation codecs which operate at data rates from 64 Kbps to 2.048 Mbps. In addition, they may have been designed using the rising clock edges for both transmit and receive data. Other aspects of these older designs could be relative skewing between the sync pulses (Data Enable) and the clock pulses in such a way that the sync pulse occurs after (Lags) the first clock pulse rising edge. All of these conditions can be easily handled using the variable data rate timing mode of the 2913/14 plus some simple external logic. By the addition of this logic, the 2913/14 becomes transparent to the older design thereby allowing an upgrade in performance while having no impact on backplane wiring or on system control hardware/software. In addition, many of the features of the 2913/14 may be incorporated, such as the test modes, which provide additional capabilities beyond those available in the original design and at a lower cost.

The circuit diagram in Figure 12 shows the maximum amount of additional random logic that could be necessary to make the 2913 or 2914 completely transparent at the linecard level (no impact on backplane wiring or timing). The inverter on $DCLK_R$ inverts all the receive clocks for each linecard. This inverter is only needed if (1) the transmit and receive clocks are inverted at the system/backplane level (as opposed to the linecard level) and (2) the previous design used only rising (or falling) edges to clock the transmit/receive data.

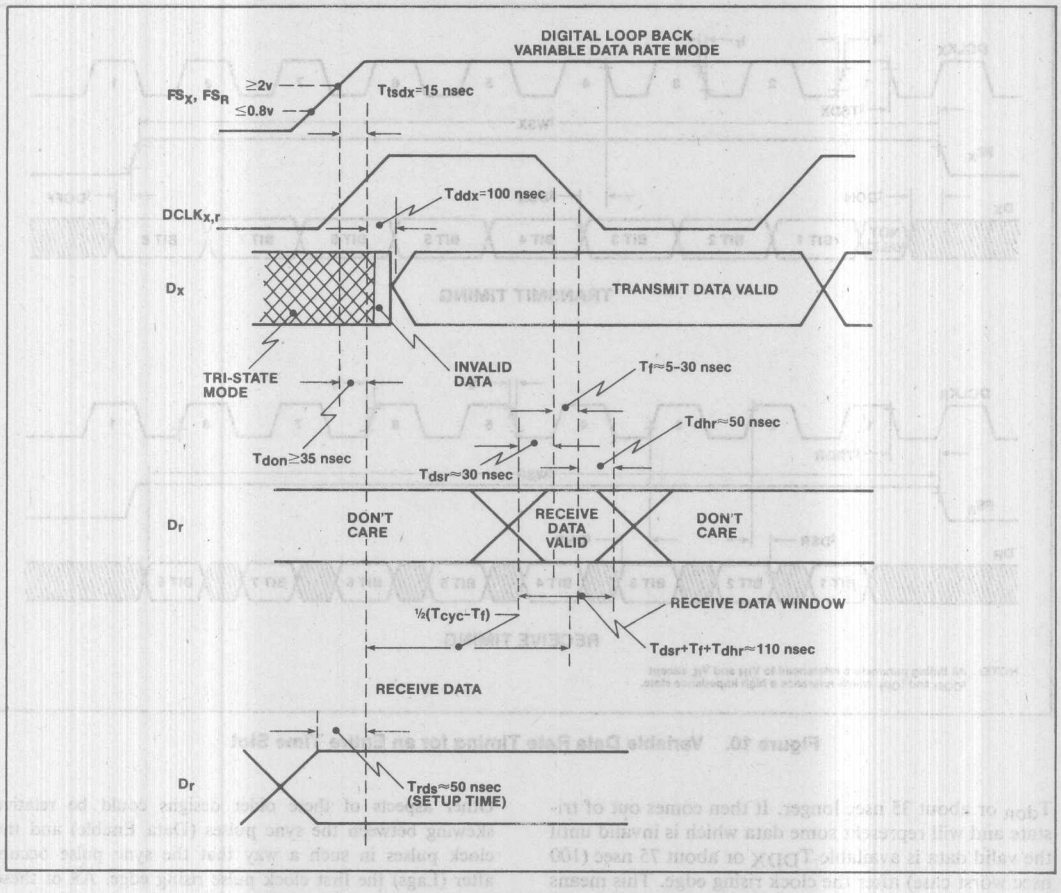


Figure 11. Waveform Timing Diagrams for the 2913/14

3.3 On-Line Test Modes

Two modes are available which permit maintenance checking of the linecard up to the SLIC/combochip interface, including the PCM highways and time slot interchanges. Tests include time slot-dependent error checking. The two test modes are called "redundancy testing" and "analog loopback." These test modes are described in detail in section 4.3.

4.0 MULTIMODE TEST CAPABILITIES

The 2913/14 was designed with every phase of design, manufacturing, and operation taken into consideration. In particular, several test modes have been implemented within the device with essentially no increase in the package size or pin count. These test modes fall into three categories: design/prototype tests, manufacturing tests, and on-line operation tests; see Table 8.

4.1 Design/Prototype Testing

In the design of a linecard prototype or in the qualification of a device, it is often helpful to have direct access to the internal nodes at key points in the LSI system. Some manufacturers even dedicate pins specifically for this function. The Intel 2913/14 approach was to reduce cost by using multifunction pins and smaller packages to achieve

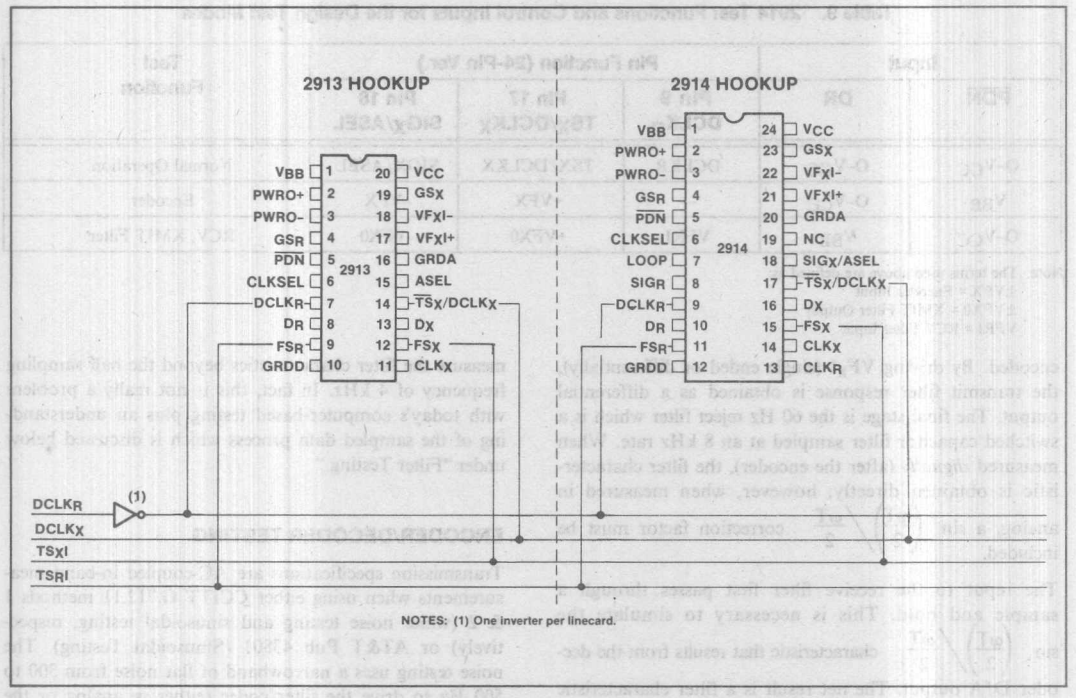


Figure 12. Circuit Diagram Showing Connections Needed to Retrofit the 2913/14 into Existing Variable Data Rate Systems

Table 8. Multimode Testing for Each Level from Design to On-Line Operation

- Design/ Prototype Testing
 - —Direct access to transmit codec inputs
 - —Direct access to the receive filter input and the transmit filter differential outputs
- Manufacturing Tests
 - —Standard half channel tests for combined codec/filters
 - —Filter response half channel measurements
- Operation On-Line Tests
 - —Analog loopback for testing PCM and codec analog highways
 - —Redundancy checks with repeatable D_X outputs

this goal. Measurements through these multipurpose pins will typically yield full device capability against performance specifications, however *these measurements are not included in the device specifications.* This is done for two reasons: first, to save manufacturing cost by eliminating unnecessary tests and specifications, and, second, more cost effective manufacturing test techniques are available, as discussed in section 4.2.

Table 9 gives the input control pin values and the corresponding functions assigned to the key test pins on the 2914 for the design test modes.

Transmit Codec (Encoder)—The transmit filter can be bypassed by directly accessing the differential input of the transmit encoder with an analog differential drive signal. Table 9 shows the control pin voltages and the input pins for this test. This test mode permits DC testing of the encoder which is otherwise blocked by the AC coupling (low frequency reject filter) of the transmit filter.

Transmit and Receive Filter—Table 9 shows the control values that permit access to the differential outputs of the transmit filter and the single-ended input to the receive filter. The voltage difference between the transmit filter outputs represents the filtered output that will be

Table 9. 2914 Test Functions and Control Inputs for the Design Test Modes

Input		Pin Function (24-Pin Ver.)			Test Function
$\overline{PDN}$	DR	Pin 9 $DCLK_R$	Pin 17 $TS_X/DCLK_X$	Pin 18 $SIG_X/ASEL$	
$O–V_{CC}$	$O–V_{CC}$	DCLKR	TSX/DCLKX	SIGX/ASEL	Normal Operation
V_{BB}	$O–V_{CC}$	—	+VFX	–VFX	Encoder
$O–V_{CC}$	V_{BB}	VFRI	+VFX0	–VFX0	RCV, XMIT Filter

Note: The terms used above are defined as:
±VFX = Encoder Input
±VFX0 = XMIT Filter Output
VFRI = RCV Filter Input

encoded. By driving VF_XI (single ended or differentially), the transmit filter response is obtained as a differential output. The final stage is the 60 Hz reject filter which is a switched capacitor filter sampled at an 8 kHz rate. When measured *digitally* (after the encoder), the filter characteristic is obtained directly; however, when measured in analog, a $\sin\left(\frac{\omega T}{2}\right)\Big/\frac{\omega T}{2}$ correction factor must be included.

The input to the receive filter first passes through a sample and hold. This is necessary to simulate the $\sin\left(\frac{\omega T}{2}\right)\Big/\frac{\omega T}{2}$ characteristic that results from the decoder D/A output. The net result is a filter characteristic that can be compared directly to the specifications.

Start-up Procedure for Test Modes—To place the 2913/14 in the test mode it is first necessary to operate the device for a few msec in normal operation. Then V_{BB} can be applied to the control pins to select the desired test access.

4.2 Production Testing

While it may be convenient for the designer to have access to both the filter and the codec inputs and outputs during the design or evaluation phase, the final product will always use the filter and codec circuits together with all signals passing through both on the way to or from the PCM highways. It therefore makes sense to perform all manufacturing measurements with the device configured in its normal operating mode, i.e., all measurements should be complete filter/codec half channel measurements. This approach not only tests the combo as it will actually be used, but also saves time and money by eliminating separate measurements and correlation exercises to determine the full half channel performance.

Since the transmission specifications of S/D, gain tracking, and ICN all require measurements which are "in-band" or "filter independent," the codec functions can be easily tested using conventional half channel measurement equipment. The apparent difficulty arises in trying to fully measure the filter characteristics beyond the half sampling frequency of 4 kHz. In fact, this is not really a problem with today's computer-based testing plus an understanding of the sampled data process which is discussed below under "Filter Testing."

ENCODER/DECODER TESTING

Transmission specifications are AC-coupled in-band measurements when using either CCITT G.712.11 methods 1 & 2 (white noise testing and sinusoidal testing, respectively) or AT&T Pub 43801 (Sinusoidal Testing). The noise testing uses a narrowband of flat noise from 300 to 500 Hz to drive the filter/codec (either in analog or the equivalent digital sequence for the transmit/receive channels, respectively). The resulting harmonic products are used to determine S/D. Likewise, gain tracking is also determined from this signal input. Sinusoidal testing uses a tone at 1.020 kHz for S/D measurements and gain tracking measurements. Idle channel noise measurements require the combined filter/codec since it has long been shown that separate measurements of filters and codecs are difficult to relate to the combined measurement (usually there is no specific relationship because of the nonlinear properties of the encoder/decoder operations). Typically the frequency response of ICN measurements is primarily determined by the weighting filter (either C message or psophometric, which are both AC-coupled, bandpass type filters).

The conclusion is that combined filter/codec testing in no way limits the measurement of half channel transmission parameters of S/D, G.T., or ICN.

FILTER TESTING

Testing the filter response, of the transmit and receive channels presents two separate test situations which, in some ways, are mirror images of one another. With the transmit side, signals may be introduced at any frequency to test the filter response. At the output of the filter, the resulting signals are sampled at 8 kHz and digitized resulting in a sequence of PCM words representing the

samples of the filtered input signal. On the receive side, a digital PCM sequence of samples representing the driving signal is converted to an analog signal by the decoder and can be measured at the filter output in analog form.

Sampling Process—In both cases of testing the filter, the signal eventually is in a sampled form. Since the sampling rate is fixed at 8 kHz, all signals must be represented below 4 kHz (half the sampling frequency). This means that the PCM bit stream can only represent signals at frequencies below 4 kHz. If a signal above 4 kHz is sampled, those samples appear exactly as if the signal was at a frequency mirror imaged about 4 kHz. Two examples include signals at 5 kHz and 7 kHz which will result in samples that look like signals of 5 – 8 kHz = 3 kHz and 7 – 8 kHz = 1 kHz, respectively.

Conversely, the sampling process produces replicas (aliasing) of the sampled signal around multiples of the sampling frequency. Therefore, if two signals are introduced digitally representing 1 kHz and 2 kHz, there will also be frequency components located at 8 kHz = ±1 kHz and 8 kHz = ±2 kHz, and so on for all multiples of 8 kHz. Thus it is possible to generate frequencies at arbitrary values after sampling by controlling the frequency of each signal within the 4 kHz input band regardless of whether it is in analog or PCM.

When an analog signal is sampled, the frequency components generated are all of the same amplitude as the corresponding input spectral components. Therefore, on the transmit side, measurements made from the PCM data will have a throughput gain of unity except where components are superimposed (e.g., a 4 kHz input signal will have an alias component at 4 kHz which may double the amplitude at 4 kHz when the two components are combined).

When an analog signal is reconstructed from digital samples, it goes through a sample and hold stage which has the effect of imposing a weighting function on the resulting spectral components that is represented by

$$\text{Sinc}\left[\frac{\omega T}{2}\right] = \frac{\text{Sin}\left(\frac{\omega T}{2}\right)}{\frac{\omega T}{2}}$$

where ω is the actual spectral component frequency going into the filter, and T is the width of the hold pulse at the decoder output. For the 2913/14, the analog output is held the full sample period of 125 μsec (1/8000 Hz) so that a frequency component at f_t will have a weighting of

$$W = \left(\frac{8000}{\pi f_t}\right) \text{Sin}\left[\frac{\pi f_t}{8000}\right]$$

Transmit Filter Test Approach—Two approaches can be used for half channel testing of the transmit filter characteristic: (1) input analog test frequencies and perform an FFT on the corresponding PCM samples that are generated to determine spectral frequencies and amplitudes at the codec output, or (2) use an "ideal" D/A converter on the PCM samples to convert the digital data back to analog so that the spectral amplitudes and frequencies can be determined using analog circuits such as spectrum analyzers or filter banks. In either case, the effects of sampling will be the same. Figure 13 shows two spectral diagrams of amplitude versus frequency. The top diagram represents the locations of nine test frequencies corresponding to the seven specified frequencies in the 2913/14 data sheet plus a component at 7 kHz and one at 10 kHz. The bottom figure shows the "equivalent" spectral component locations when carried in the PCM bit stream. As an example, frequency #8 is located at 7 kHz. The corresponding PCM frequency is seen in the lower figure at 1 kHz. Note also that the analog component at 9 kHz (see #8*) would also generate the 1 kHz component in the PCM data.

To test the filter, the desired test frequencies are introduced in analog to the filter input in such a way that there is no confusion as to where the resulting component will be after sampling (i.e., don't simultaneously put in 1 kHz and 7 kHz since both of these inputs result in a 1 kHz component in the PCM data). Then, using either technique (FFT or analog) mentioned above, measure the amplitude of the corresponding sampled component. The

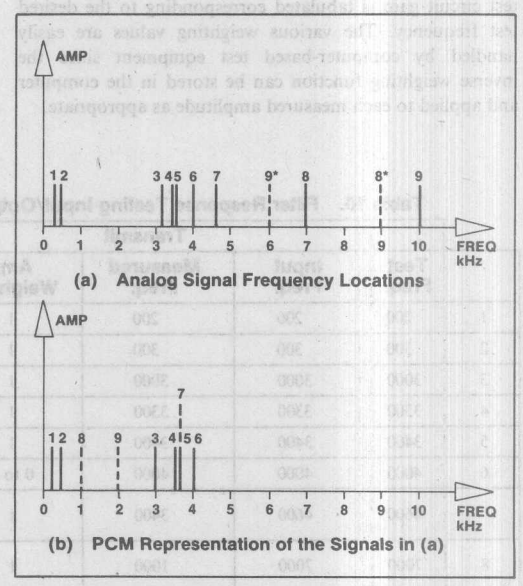


Figure 13. Spectral Properties of the Filter Test Frequencies in Analog and PCM

difference between that amplitude and the input amplitude represents the filter attenuation *at the frequency of the input signal.* So, if the input signal was at 7 kHz, the FFT will determine the amplitude of the corresponding 1 kHz signal. The amplitude change relative to the input will represent the filter attenuation at 7 kHz.

Receive Filter Test Approach—In this case, the PCM test signals can be generated directly from digital circuits or by going through an "ideal" A/D (companded) to generate the PCM samples. Since these samples represent frequencies below the half sampling rate, Figure 12(b) now represents the input signals and 12(a) the output, but with one significant difference—a Sinc[π f_I/8000] weighting function is imposed on all the frequency components because of the decoder sample and hold output. At the filter output, the spectral component amplitudes will include the effect of the filter response *and* the weighting function measured at the actual test frequency. The receive filter includes a compensation network for the weighting function in its passband. Therefore, inside the passband (300 Hz to 3.4 kHz) the measured amplitudes should be compared directly to the data sheet specifications. Frequencies outside the passband must be compensated for the weighting function first to determine the true filter response.

Summary of Filter Testing—Table 10 lists the nine test frequencies shown in Figure 12 for both the transmit and receive filter testing. For each filter test, the input frequency (analog or PCM), measurement frequency, and test circuit gain is tabulated corresponding to the desired test frequency. The various weighting values are easily handled by computer-based test equipment since the inverse weighting function can be stored in the computer and applied to each measured amplitude as appropriate.

4.3 Operational On-Line Testing

Two test modes are available which facilitate on-line testing to verify operation of both the combochip and the entire switching highway network. The first is simply the capability to duplicate the same D_X transmission in multiple PCM time slots (redundancy checking), and the second is the analog loopback capability which allows the testing of a call completion through the entire PCM voice path including the time slot interchange network.

Redundancy Checking—A feature of the 2913/14 is that the same 8-bit PCM word can be put on the D_X highway in multiple time slots simply by holding the frame sync/data enable (FS_X) high and continuing to supply clock pulses (CLK_X or $DCLK_X$). If the data enable was held high for multiple time slots, each time slot would have identical data in it. By routing this data through the PCM highways, time slot interchanges, etc., and then correlating the data between time slots, it would be possible to detect time slot-dependent data errors. When this test mode is used, no other data will be generated for the transmit highway until the frame sync returns low for at least one full clock cycle.

Analog Loopback—The 2914 (2913 does not have this feature) has the capability to be remotely programmed to disconnect the outside telephone lines and tie the transmit input directly to the receive output to effect analog loopback within the combo chip. This is accomplished by setting the LOOP input to V_{CC} (TTL high). The result is to disconnect VF_XI+ and VF_XI- from the external circuitry and to connect internally PWRO+ to VF_XI+, GS_R to PWRO–, and VF_XI- to GS_X (see Figure 14).

With this test set up, the entire PCM and analog trans-

Table 10. Filter Response Testing Input/Output Frequencies and Amplitude Gain Schedule

		Transmit			Receive		
	Test Freq.	Input Freq.	Measured Freq.	Amp Weighting	Input Freq.	Measured Freq.	Amp Weighting
1	200	200	200	1	200	200	1
2	300	300	300	1	300	300	1
3	3000	3000	3000	1	3000	3000	1
4	3300	3300	3300	1	3300	3300	1
5	3400	3400	3400	1	3400	3400	1
6	4000	4000	4000	0 to 2	4000	4000	0 to 2
7	4600	4600	3400	1	3400	4600	$\text{Sinc}\left[\frac{4600\ \pi}{8000}\right]$
8	7000	7000	1000	1	1000	7000	$\text{Sinc}\left[\frac{7000\ \pi}{8000}\right]$
9	10000	10000	2000	1	2000	10000	$\text{Sinc}\left[\frac{10000\ \pi}{8000}\right]$

mission path up to the SLIC can be tested remotely by assigning a PCM word to a time slot that is read by the combo being tested. This data is converted to analog and passed out of the receive channel. It is taken as input by the transmit channel where it is filtered and re-digitized (encoded) back to PCM. The PCM word can now be put on the transmit highway and sent back to the remote test facility. By comparing the PCM data (individually or as a series of codes) the health of that particular connection can be verified.

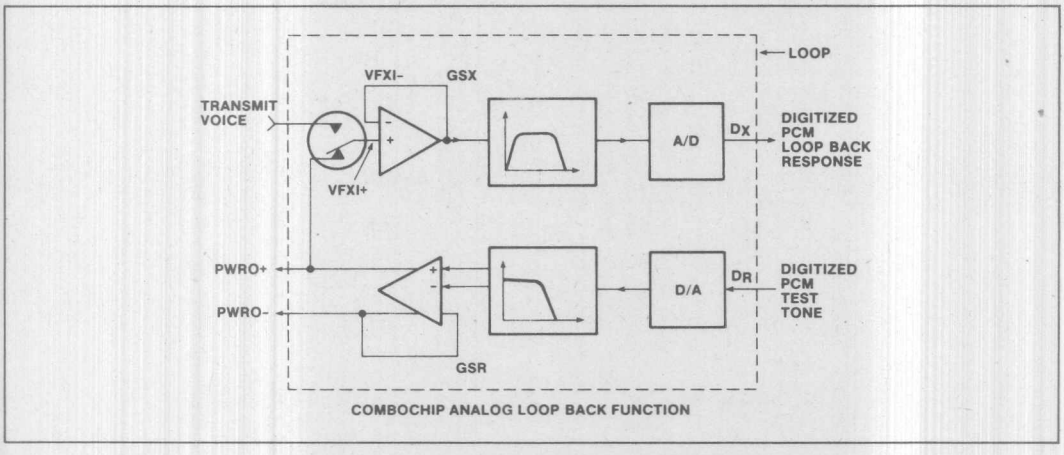
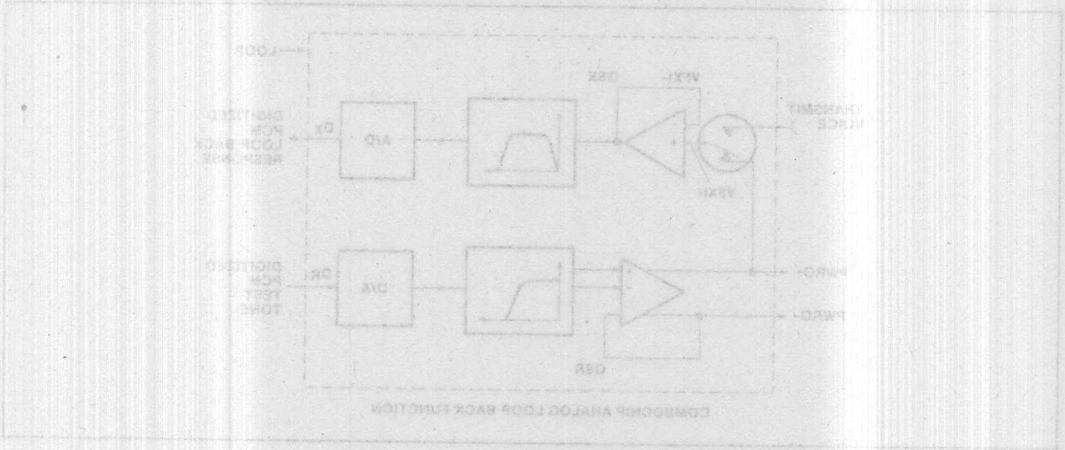


Figure 14. Simplified Block Diagram of 2914 Combochip in the Analog Loopback Configuration



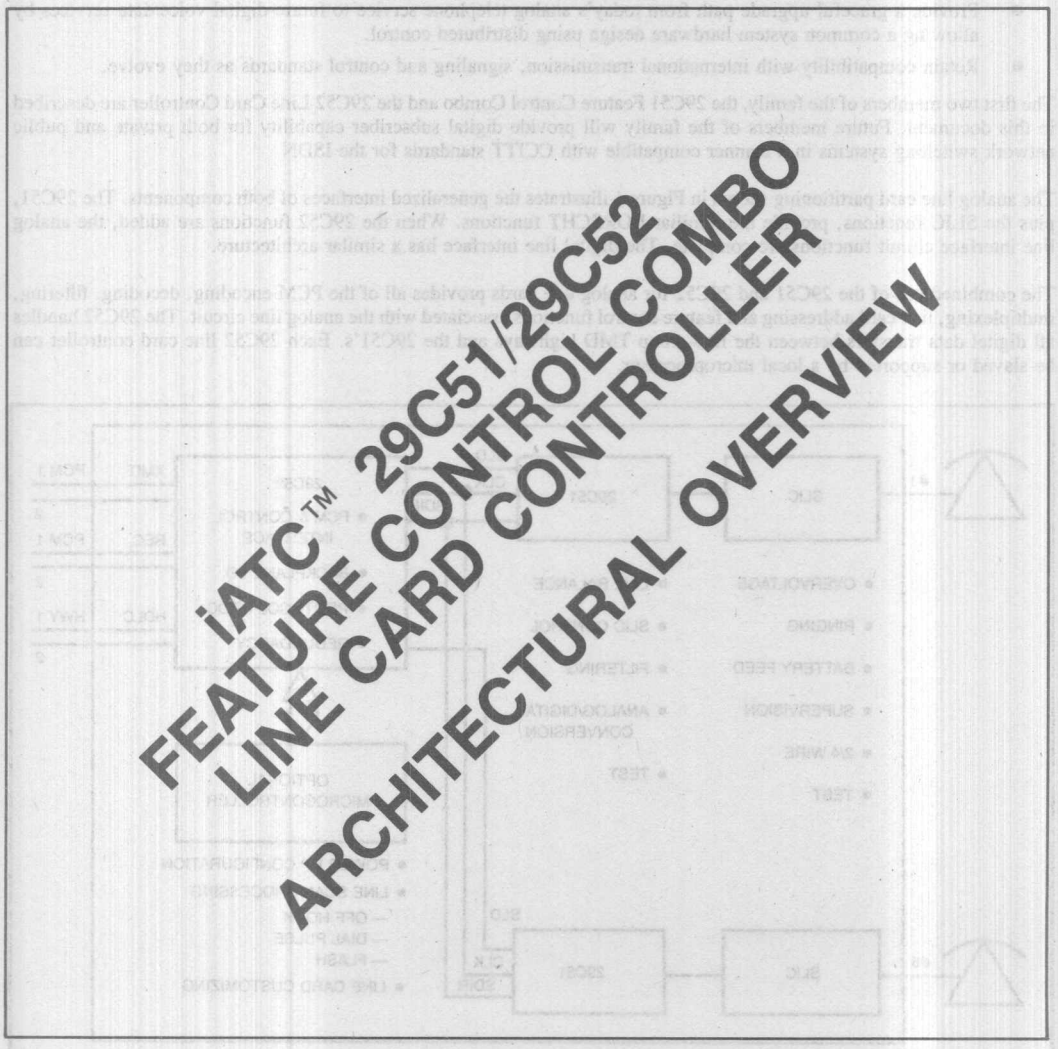
iATC™ 29CX Advanced Telecommunications Components

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March 1983

iATC™ 29C51/29C52 FEATURE CONTROL COMBO LINE CARD CONTROLLER ARCHITECTURAL OVERVIEW



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Order Number 210930-001

Intel is developing a family of advanced telephony line-interface circuit components which give OEM's an evolutionary growth path toward an all-digital network. These new VSLI devices fit into system architectures which are flexible enough to support both analog and digital subscriber lines.

These components are based on the following design philosophy:

- Integrate as much of the low-voltage, per-line functions of the analog line circuit as is cost effective.
- Support an all-serial backplane bus architecture for digital TDM highways, signaling and control buses, and line-card addressing.
- Add a wide variety of per-line features to the normal BORSCHT functions for the analog line circuit.
- Make analog and digital subscriber line circuit cards plug-compatible in a line equipment shelf.
- Allow all system transmission, signaling, and control buses to serve analog and/or digital subscriber lines, or analog trunks, interchangeably.
- Provide a graceful upgrade path from today's analog telephone service to future digital voice/data services by allowing a common system hardware design using distributed control.
- Retain compatibility with international transmission, signaling and control standards as they evolve.

The first two members of the family, the 29C51 Feature Control Combo and the 29C52 Line Card Controller are described in this document. Future members of the family will provide digital subscriber capability for both private and public network switching systems in a manner compatible with CCITT standards for the ISDN.

The analog line card partitioning shown in Figure 1 illustrates the generalized interfaces of both components. The 29C51, plus the SLIC functions, provide the familiar BORSCHT functions. When the 29C52 functions are added, the analog line interface circuit functions are complete. The digital line interface has a similar architecture.

The combined use of the 29C51 and 29C52 for analog line cards provides all of the PCM encoding, decoding, filtering, multiplexing, line card addressing and feature control functions associated with the analog line circuit. The 29C52 handles all digital data transfers between the line-group TMD highways and the 29C51's. Each 29C52 line card controller can be slaved or supported by a local microprocessor.

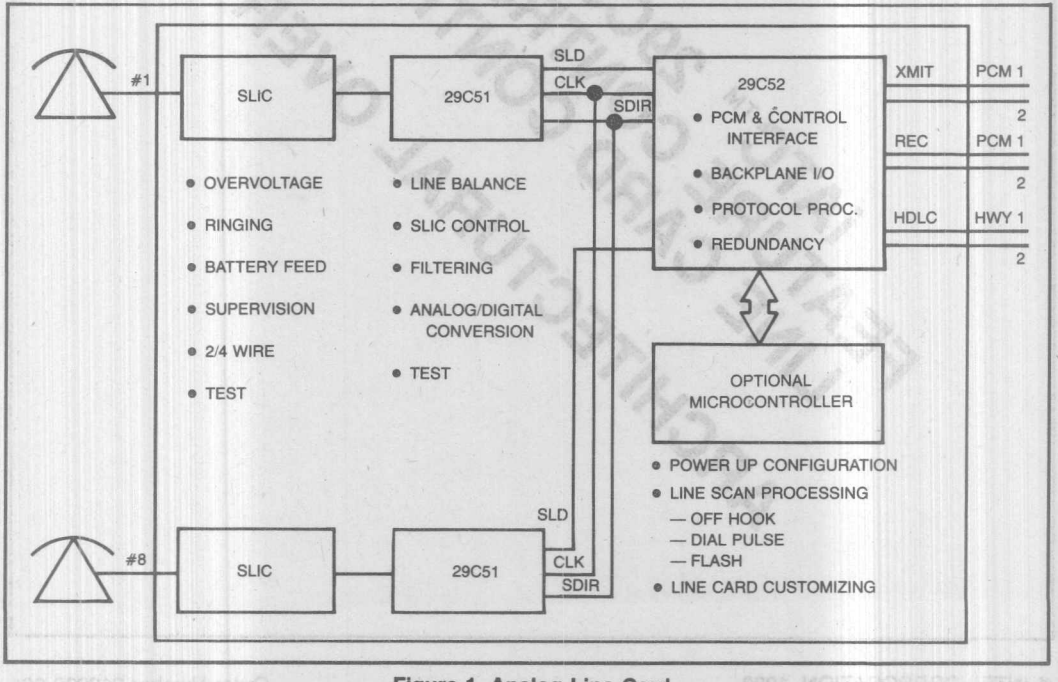


Figure 1. Analog Line Card

PRELIMINARY

iATC
29C50 and 29C51
FEATURE CONTROL COMBO

- **29C50 22-pin, 7 signaling channels**
- **29C51 28-pin, 10 signaling channels, secondary analog inputs and outputs**

- **External and User Programmable Transmit and Receive Gain**
- **Programmable Internal and External Hybrid Balance Network Select**
- **Programmable Analog, Digital, and Subscriber Loopback**
- **Programmable μ/A-Law Select**
- **Flexible Signaling Interface**
- **Secondary Analog Channel**
- **Three-Party Conferencing**
- **Low Power Consumption**

The Intel iATC 29C50/29C51 Feature Control Combo is an advanced user-probrammable, fully integrated PCM Codec with transmit/receive filters fabricated in a CMOS technology. This technology is built on CHMOS and will allow the 29C50 and 29C51 to realize the same excellent transmission performance as in the Intel 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C50/29C51 are the first members of Intel's third generation advanced telecommunication components. The Feature Control Combo supports the analog subscriber with a variety of added per-line features to the normal BORSCHT functions associated with the analog line circuit. Some of these features include secondary analog channels, programmable transmit and receive gain, on-chip or custom hybrid balancing network selection, a flexible signaling interface, and programmable μ or A-law conversions.

The 29C50/29C51 is intended for use with the 2952 Integrated Line Card Controller in digital switching environments. These components allow the system transmit and receive backplane highways to operate at different frequencies from that of the subscriber interface data channels. The 2952 handles the transfer of primary voice, secondary analog data, feature control, and signaling information between the backplane and up to 8 29C50/29C51's.

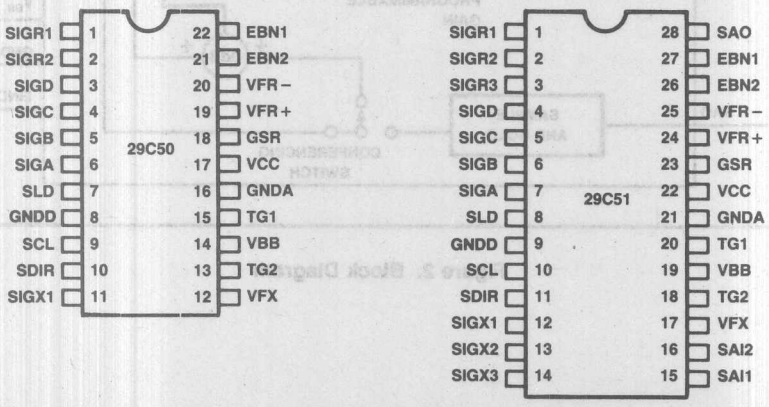


Figure 1. Pin Configuration

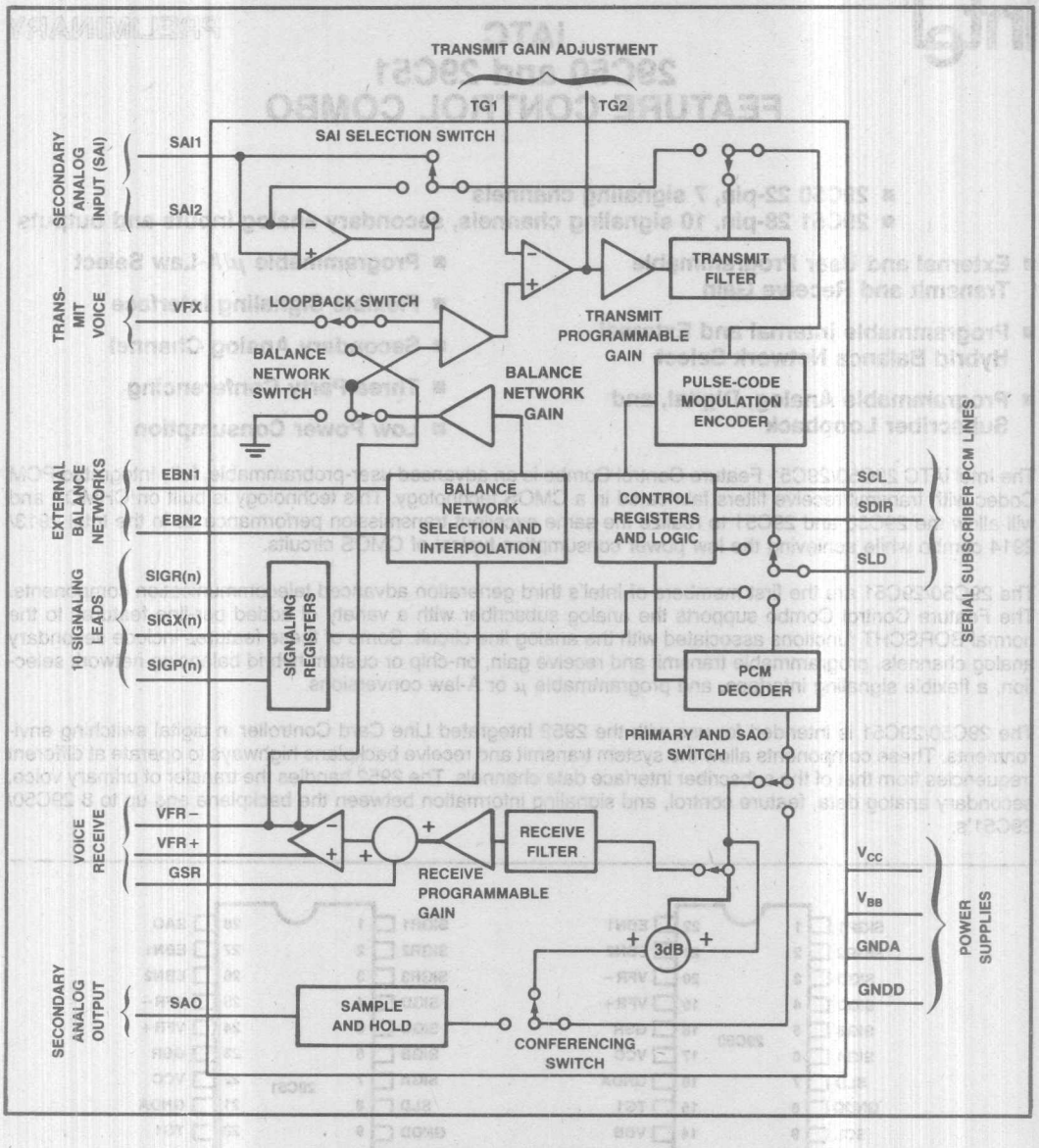


Figure 2. Block Diagram

Table 1. Pin Names

VFX	Analog Input	SCL	Subscriber Clock
VFR+, VFR−	Analog Output	SLD	Subscriber Data Link
SAI1, SAI2	Secondary Analog Inputs	SDIR	Subscriber Direction
SAO	Secondary Analog Output	TG1, TG2	Transmit Gain Adjust
GNDD	Digital Ground	GSR	Receive Gain Adjust
GNDA	Analog Ground	EBN1, EBN2	External Balance Network
V_{CC}	Power (+5V)	SIGX1, X2, X3	Transmit Signaling Input
V_{BB}	Power (−5V)	SIGR1, R2, R3	Receive Signaling Output
		SIGA, B, C, D	Programmable Transmit/ Receive Signaling Lead

Table 2. Pin Description

Symbol	Function
VCC	Most positive supply; input voltage is +5V±5%.
VBB	Most negative supply; input voltage is −5V±5%.
GNDA	Analog ground return line. Not internally connected to GNDD.
GNDD	Digital ground return line. Not internally connected to GNDA.
VFX	Analog voice input to transmit channel.
TG1	Inverting input to transmit gain adjusting op-amp. Feedback point for external gain adjusting resistor network up to 10k ohm.
TG2	Output of the transmit gain adjusting op-amp. Will drive external gain adjusting resistor network up to 10k ohm.
VFR+	Non-inverting output of the power amplifier. Capable of directly driving transformer hybrids or high impedance loads either single ended or differentially.
VFR−	Inverting output of power amplifier. Capable of directly driving transformer hybrids or high impedance loads either single ended or differentially.
GSR	Input to receive gain setting circuit. An external resistor network connected between VFR− and VFR+, and GSR sets the receive channel gain from 0dB to −9.54dB. Connecting GSR to GNDA will set the gain at −6.02dB.
EBN1	Input for the first external balance network.
EBN2	Input for the second external balance network.
SAI1	First secondary analog input, also the non-inverting input if differential secondary analog input mode is selected.
SAI2	Second secondary analog input, also the inverting input if differential secondary analog input mode is selected.

Symbol	Function
SAO	Secondary analog output, capable of driving loads of a least 10kΩ.
SCL	Subscriber clock. Supplied by the 2952 line card controller, this is a 512 kHz, 50% or 33% duty cycle clock. Input will accept TTL levels.
SDIR	Subscriber direction signal and frame sync. When high, SLD becomes an input and data is transferred from the 2952 to the 29C51. When low, the output buffer on the 29C51 SLD pin is enabled and data is transferred from the 29C51 to the 2952. Input will accept TTL levels.
SLD	Subscriber data link. A 512kbps bi-directional serial data port, which is clocked by SCL. SLD becomes a TTL compatible input when SDIR is high and an output capable of driving one TTL load when SDIR is low.
SIGX1 SIGX2 SIGX3	Transmit signaling inputs. Data present at SIGX(n) is latched by an internal signal preceding the falling edge of SDIR and is serially transferred on SLD during the transmit signaling byte. TTL compatible.
SIGR1 SIGR2 SIGR3	Receive signaling outputs. Data received serially on SLD during the receive signaling byte is latched on these outputs during the following byte. Capable of driving one TTL load.
SIGA SIGB SIGC SIGD	Programmable signaling pins. If the appropriate bit in the feature control memory is set high (either SIGDA, SIGDB, SIGDC, or SIGDD), the corresponding pin will become a receive signaling output, like SIGR(n). If the bit in the feature control memory is set low, the corresponding pin will become a transmit signaling input, like SIGX(n). Inputs will accept TTL level inputs, and outputs can drive one TTL load.

FUNCTIONAL DESCRIPTION

The 29C50/29C51 is a combined channel filter and PCM codec for use on analog line interface circuit boards in a digital telecommunications switching system. This device resides between the circuitry which provides the "BORSHT" functions for a given line, and the shared line board controller. It provides the transmit and receive voice-path filtering and companded analog-to-digital and digital-to-analog conversions necessary to interface a full duplex (4-wire) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

All features of the 22-lead device (29C50) are identical to that of the 28-lead device (29C51) except for the number of signaling pins and the secondary channel capabilities. There are 10 signaling channels available on the 29C51 configured as three transmit, three receive, and four programmable for either direction. Seven signaling leads are located on the 29C50 providing one transmit, two receive, and four programmable. There are no secondary analog inputs or outputs on the 29C50, however, three-party conferencing is still available.

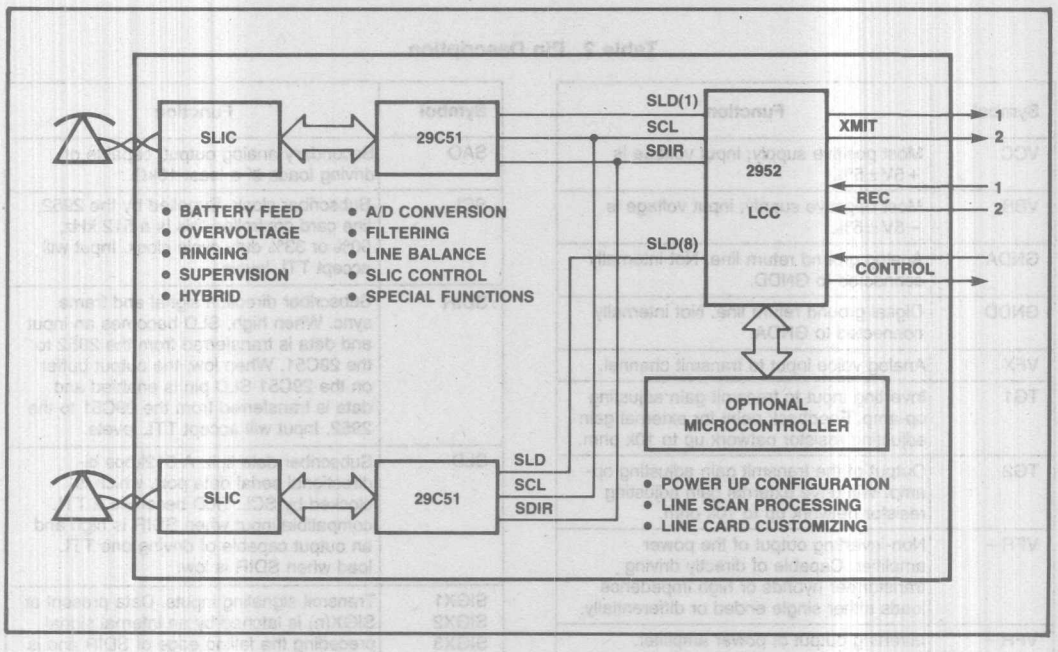


Figure 3. Analog Linecard

TRANSMIT AND RECEIVE OPERATION

Transmit Filter

A low pass anti-aliasing section is included on chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 specification and the CCITT G.712 recommendation. The 29C50 and 29C51 specifications meet the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 10.

A high pass section configuration rejects low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Gain of up to 20dB can be set without degrading the performance of the filter.

Encoding

The output of the transmit filter is internally sampled by the encoder and held on an internal sample and hold capacitor. DC offset is corrected by an on-chip auto zero circuit. The signal is then encoded and presented as PCM data on the SLD lead on the first 8 bits of the XMIT half frame (fifth byte). Secondary analog input signals are routed directly to the encoder and output in the sixth byte on the SLD.

Decoding

The PCM words received on the SLD are demultiplexed and sent to the decoder. The decoded value is held on an internal sample and hold capacitor. If the secondary analog channel is being used, the PCM word received in the second byte on the SLD is decoded, then held on another sample and hold capacitor before appearing on the secondary analog output (SAO). If, however, conferencing has been selected, the two converted signals will be added and subsequently passed to the receive filter.

Receive Filter

The receive section of the filter provides a passband flatness and stopband rejection which fulfills the AT&T D3/D4 specification and the CCITT G.712 recommendation. The receive filter transfer characteristics and specifications will be within the limits shown in Figure 11.

GENERAL OPERATION

External Gain Setting

Both transmit and receive gain levels are factory trimmed, but can be modified by external resistors during line card assembly. The value of transmit gain is adjusted by connecting resistors RT1 and RT2 (see Figure 4) at the two external gain setting control pins, TG1 and TG2. These two pins are the input and output of an on-board gain amplifier stage, and the resistors provide the necessary input and feedback for gain control. The value of external gain is given by:

$$A = 1 + RT1/RT2$$

For unity gain, pins TG1 and TG2 are tied together. Similarly, for the receive section, external resistors RR1 and RR2 at pins VFR+, GSR, and VFR− set the external gain given by:

$$A = (RR1 + RR2)/(RR1 + 3RR2)$$

A value greater than 10k ohms and less than 100k ohms for R1 + R2 is recommended. The output is capable of driving loads of 300 ohms at 3.2Vp single ended or 600 ohms at 6.4Vp differentially.

Three additional gain settings of 0dB, −6dB, and −9.54dB can be realized without using any external components by strapping pin GSR to VFR−, GNDA, and VFR+, respectively.

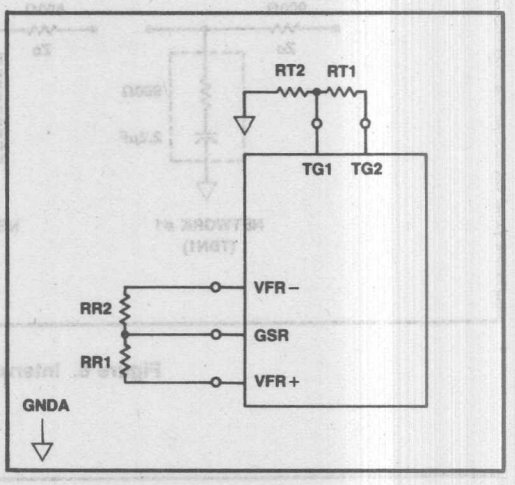


Figure 4. External Gain Connections

Hybrid Balancing Network

The 2- to 4-wire conversion necessary for subscriber interface is partially integrated on-chip. Network line balancing needed to minimize the trans-hybrid loss from the receive to transmit direction analog signals is handled internally. The three internal networks shown in Figure 6 may be selected by programming the appropriate feature control byte. These networks are integrated in a switched capacitor configuration and have single pole-zero characteristics in the 200 Hz to 3200 Hz range. They were chosen to serve a wide base of U.S. and European requirements, and can be used as standard line balancing networks or as test networks.

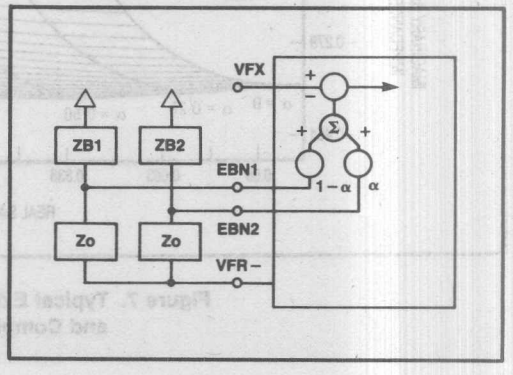


Figure 5. External Balance Network and Interpolation Configuration

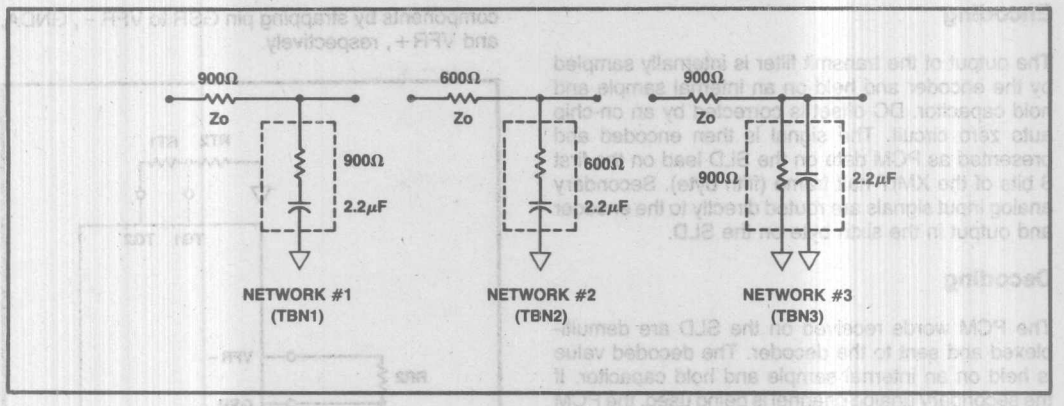


Figure 6. Internal Balance Networks

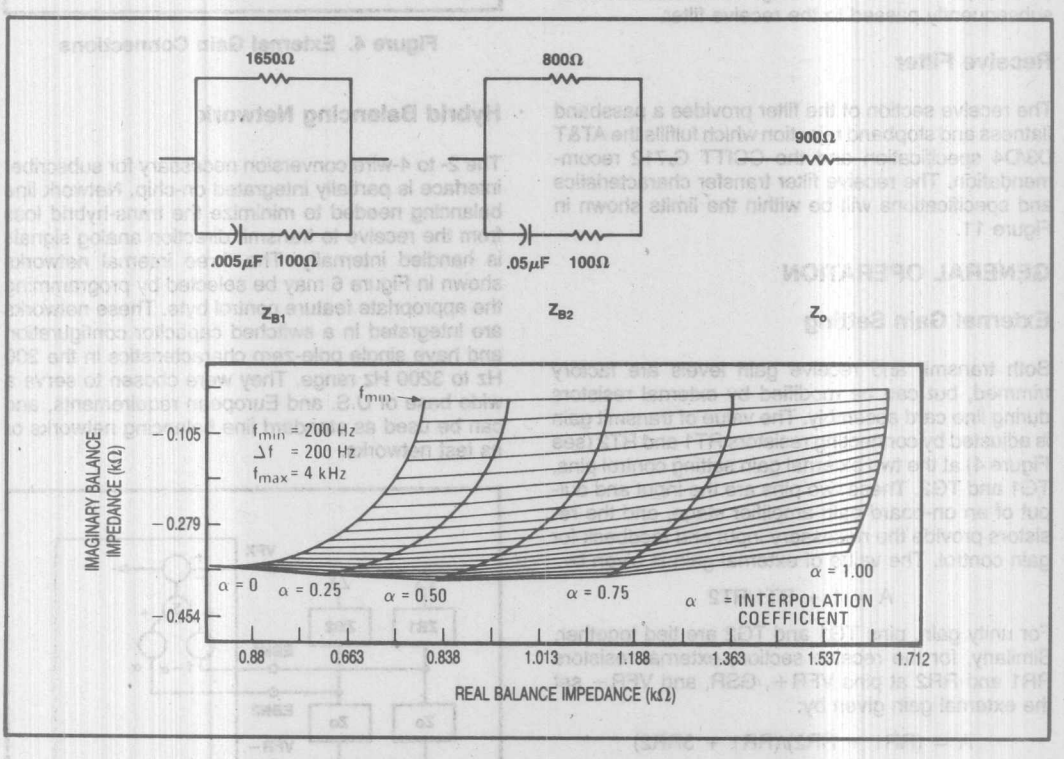


Figure 7. Typical External Balance Networks and Complex Impedance Plot

Additionally, the user may apply two external balance networks to accommodate varying subscriber loop characteristics (See Figure 5 for external connections). Presumably, these two networks can represent the two extremes of line conditions in different applications such as long or short loops and loaded or unloaded lines. To serve typical lines with characteristics in between the two extremes, the interpolation capability provides a weighted average of the network frequency characteristics. If the external network at EBN1 produces a transfer function $H1(f) = ZB1 (Zo + ZB1)$ and the network at EBN2 produces $H2(f) = ZB2 (Zo + ZB2)$, the balance signal can be programmed to have the transfer function H(f):

$$H(f) = \alpha\, H1(f) + (1-\alpha)\, H2(f)$$

where "α" is the interpolation coefficient programmed to have any of the five values of 0, .25, .50, .75, or 1.0. Figure 5 displays how the subtraction of the coupling signal is implemented inside the device.

As an example, the two external networks shown in Figure 7 represent typical hybrid balance networks for loaded (ZB1) and unloaded (ZB2) analog loops. The graph in Figure 7 shows the real and imaginary components of the equivalent impedance of these two networks as a function of frequency and the interpolation coefficient.

Secondary Analog Channel/Conferencing

The 29C51 offers two simultaneous unfiltered information channels beyond the primary channel. Narrow band analog signals can be supplied for such applications as telemetry, teleconferencing, remote loop testing, or various control uses.

The secondary analog channel is accessed through two inputs, SAI1 and SAI2, sampled either single ended or differentially. The unfiltered secondary analog output, SAO, is a stair-step signal with the inherent sinx/x frequency rolloff following D/A conversion.

To allow three-party conferencing, the third party voice information can be transmitted and received during the data bytes carrying the secondary analog channel information. The primary and secondary voice signals are held on separate internal capacitors following D/A conversion, then passed through a −3dB attenuator and summed together. The combined signal is smoothed in the receive filter and passed onto the output power amplifier.

Precision Voltage References

Voltage references are generated on-chip and are trimmed during the manufacturing process. Separate references are supplied for both the transmit and receive sections of the chip, each trimmed independently. These references determine the gain and dynamic range of the device and provide the user a significant margin for error in other board components.

SLD Interface

The 29C50 and 29C51 are intended for use with the 2952 Line Card Controller which manages the transfer of all voice, feature control and signaling data to and from the Feature Control Combo and the system backplane. The interface between the two consists of just three leads, two of which are clock signals and the third a unique serial bus for communication. Up to eight 29C50/29C51 feature control combos per line card can be controlled by one 2952, all sharing common clock signals, SCL and SDIR.

The subscriber direction (SDIR) lead provides an 8 kHz signal which divides each frame into transmit and receive halves. During the first half when SDIR is high (RCV half-cycle), data is transmitted from the 2952 to the 29C51 and in the second (XMIT half-cycle) transfer is from the 29C51 back to the 2952. Frame synchronization and all internal timing for the digital circuitry is derived from the rising edge of the SDIR signal.

The subscriber clock (SCL) input generated by the 2952 is a fixed 512 kHz clock signal allowing 64 bits (8 bytes) of data to be transferred on the SLD lead during each 125 μsec frame. Depending on 2952 master clock frequency, the SCL duty cycle can be either 50% or 33%.

The subscriber data link (SLD) is a bidirectional serial bus that transfers eight bytes of serial data to and from the 29C51 each frame. During the first half of each frame, RCV channel information is transferred to the 29C51 in four bytes consisting of voice, data, feature control, and signaling information. (The data byte actually contains the secondary analog channel information.) Similarly during the second half-cycle, four bytes of XMIT channel information are sent to the 2952. The MSB (bit 7) of each byte is sent first on the SLD. After the last valid signaling bit is transmitted to the 2952, the bus is placed in a high impedance state for at least one SCL clock cycle to prevent data contention on the bus. (See FCB#6—Signaling Register)

Upon power supply application and clocks SCL and SDIR applied, the 29C51 will automatically enter the power down state. During the transmit half cycle (29C51 talking to the 2952) a code of all ones will be sent to the controller during the VOX and DAX bytes.

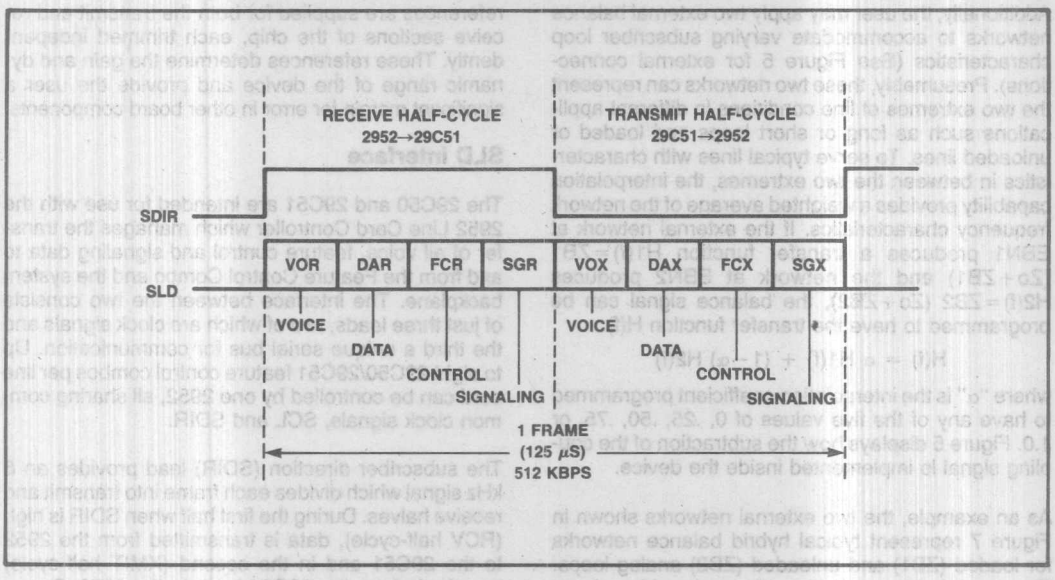


Figure 8. 29C51/2952 Interface

PROGRAMMABLE FEATURES

The 29C51 is configured by the 2952 line card controller by a set of six feature control bytes (FCB). These bytes of information are stored in internal registers which are serially multiplexed to and from the SLD interface in the third and seventh byte locations. The first two bits of each byte consist of a multiframe synchronization and write enable code. The framing bit (bit 7, MSB) establishes the beginning of a feature control frame when set to a logical zero, and increments the feature control counter when set to one. The second (bit 6) enables the writing to the 29C51 when it is the logical complement of the framing bit.

When writing new feature control information to the 29C51, the first byte should contain a framing (F) and write enable (WE) header of 01 (F = 0 and WE = 1). This designates a new frame of information to transfer. The subsequent bytes should each have F = 1 to advance the counter, and WE = 0 to enable the write operation.

The controller can also request to verify the feature control register contents by sending a 00 or 11 at the beginning of the byte to be read. To read the first byte, a 00 F/WE code should be sent while each subsequent byte should have a 11 header. An internal six-stage counter is set on the first byte verified then incremented once each 125μs frame. It is reset only upon detection of a 01 or 00 F/WE. Once the counter is greater than six, neither read nor write modes may be selected by sending the 29C51 a 11 framing and write enable code. The 29C51 will then echo in byte 7 the data it received in byte 3.

FCB #1 — Power Up/Down, Loop Back Mode, μ/A-Law Select Register

POWER UP AND DOWN

The 29C50/29C51 can be instructed to go into the power down or standby mode for reduced power consumption. In this mode, all analog inputs and outputs are placed in a high impedance state, inhibiting all primary voice and secondary data signals. A code of all ones will be output in the voice and data bytes on the SLD. Signaling and feature control information will continue to be processed to allow the 29C51 to be read or reprogramed, and to allow the backplane to monitor the subscriber line.

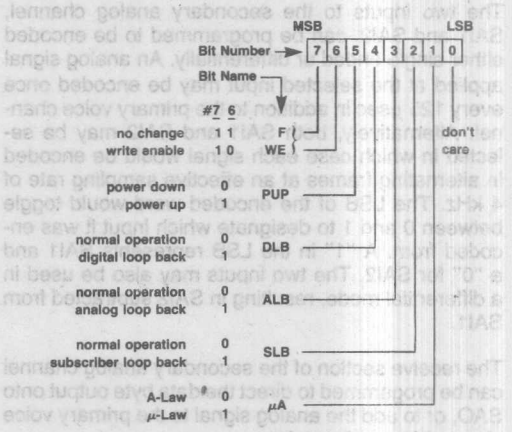
The 2952 can change the state of the feature control combo from standby to active by sending the first feature control byte only. All other register contents will be preserved during power down provided the power supplies remain connected.

LOOP BACK MODE SELECT

Three modes of remote testing are incorporated in the 29C50/51 and can be selected by appropriate coding in this register. The loopback features allow a number of tests to be performed to determine line quality and balancing. These include digital loop back, analog loop back, and subscriber loop back.

In the digital loopback mode, the combo retransmits the PCM words it receives in the voice and data bytes of the SLD back to the line card controller in the same frame. This feature allows path verification and testing of the circuit up to the slave device.

When the analog loopback mode is selected, the analog output VFR+ is internally connected to the analog input VFX. This feature allows functional testing of the combo as well as gain adjustment. The secondary analog channel is unaffected during this operation.



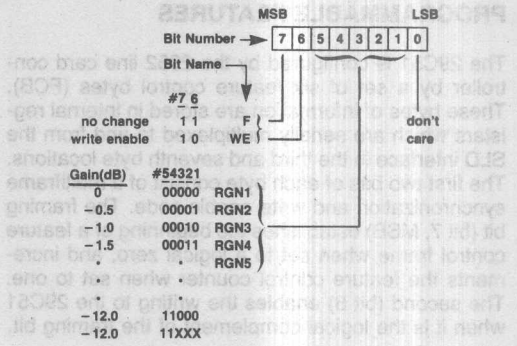
In the third test mode, subscriber loopback, the digital output of the A/D converter is internally connected to the input of the D/A converter. The analog signal input to VFX is sent through the transmit filter, encoded, then decoded, filtered and output to VFR+ and VFR−. This mode is used primarily for simplifying analog to analog testing from the subscriber side of the line card. If the secondary analog inputs and output are being used, they will be looped back in the same manner.

CONVERSION LAWS

The 29C50 and 29C51 can be selected for either μ-law or A-law operations. A user can select either conversion law by assigning the corresponding bit. A logical 1 in bit 1 would select μ-law while a logical 0 would select A-law conversions. Both conversions follow CCITT recommendation G.711.

FCB #2 — Receive Programmable Gain Register

The receive gain levels can be adjusted by applying external resistors as mentioned earlier, or by selective programming of this register. A range from 0 to −12dB in 0.5dB increments can be realized for the receive channel.

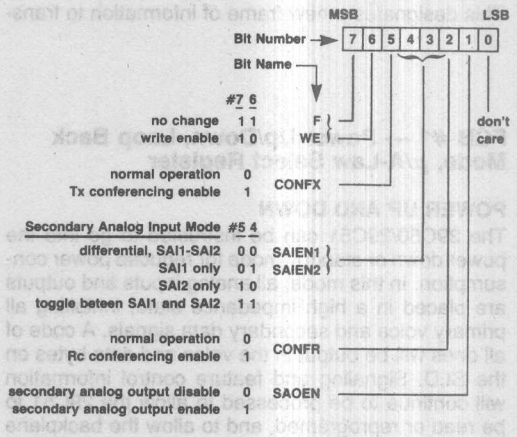


FCB #3 — Secondary Analog Channel Register

SECONDARY ANALOG INPUTS AND OUTPUTS

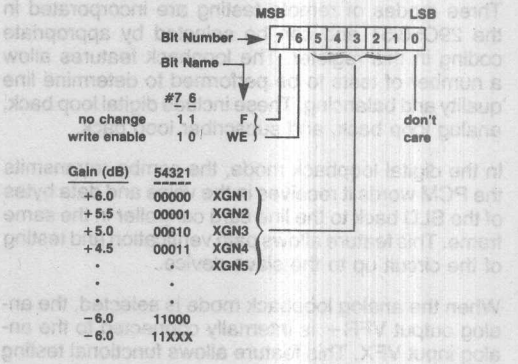
The two inputs to the secondary analog channel, SAI1 and SAI2, can be programmed to be encoded either single ended or differentially. An analog signal applied at the selected input may be encoded once every 125 μsec in addition to the primary voice channel. Alternatively, both SAI1 and SAI2 may be selected in which case each signal would be encoded in alternating frames at an effective sampling rate of 4 kHz. The LSB of the encoded word would toggle between 0 and 1 to designate which input it was encoded from. A "1" in the LSB represents SAI1 and a "0" for SAI2. The two inputs may also be used in a differential mode, resulting in SAI2 subtracted from SAI1.

The receive section of the secondary analog channel can be progammed to direct the data byte output onto SAO, or to add the analog signal to the primary voice channel for conferencing.



FCB #4 — Transmit Programmable Gain Register

The gain setting of the transmit section of the chip operates in the same manner as the receive gain register. A 12dB range from −6.0dB to +6.0dB in 0.5dB increments is available.



FCB #5 — Balance Network Select and Gain Register

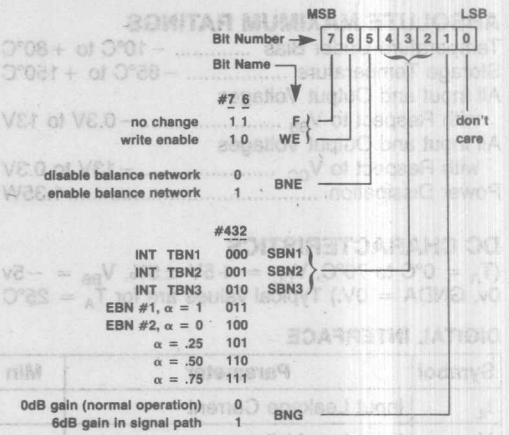
BALANCE NETWORKS

The 29C51 offers a choice of internal or external hybrid balancing. Externally, two balance networks connected to pins EBN1 and EBN2 can be used independently, or as a weighted average of the two. The weighting factor, or interpolation coefficient, can range from 0 to 1 in steps of .25. Setting "α" to be 1 or 0 results in selecting either EBN1 or EBN2 respectively.

Three additional balance network configurations consisting of either a series or parallel RC circuit are located internal to the device. (See Figure 6).

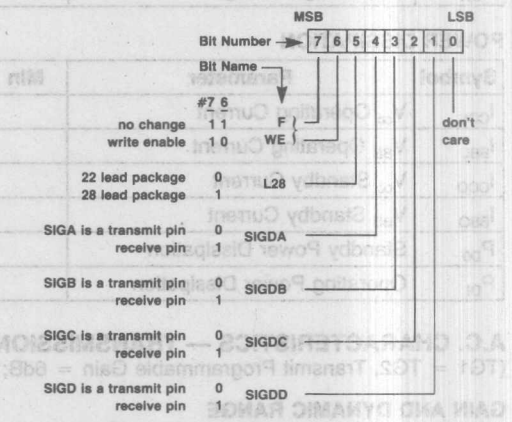
GAIN SETTING

An additional 6dB gain in the balance signal path can be realized by coding this bit with a logical one. A logical zero provides unity gain.



FCB #6 — Signaling Register

Four pins are provided on both the 29C50 and 29C51 chips to be used as selectable transmit or receive signaling inputs. A code of one in the respective bit commits the pin to receive signal information and a zero to transmit. The signaling field format as it appears on the SLD bus is shown in Figure 9 for both the 29C50 and 29C51. R1, R2, and R3 correspond to signaling information received on SIGR1, SIGR2, and SIGR3 respectively. Similarly, programmable pins SIGA, SIGB, SIGC, SIGD, and transmit pins SIGX1, SIGX2, SIGX3 are coded into the bit location as shown below.



Receive Signaling SLD Byte #4

Bit	MSB 7	6	5	4	3	2	1	LSB 0
29C51:	R1	R2	R3	A	B	C	D	—
29C50:	R1	R2	A	B	C	D	—	—

Transmit Signaling SLD Byte #8

Bit	MSB 7	6	5	4	3	2	1	LSB 0
	X1	X2	X3	A	B	C	D	Z
	X1	A	B	C	D	Z	Z	Z

Z = High Impedance State
— = Don't Care State

Figure 9. Signaling Field Format

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias −10°C to +80°C
Storage Temperature −65°C to +150°C
All Input and Output Voltages
with Respect to V_{BB} −0.3V to 13V
All Input and Output Voltages
with Respect to V_{CC} −13V to 0.3V
Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = −5v ±5%; SCL (50% duty), SDIR, SLD applied GNDD = 0v, GNDA = 0V.) Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Leakage Current			±10	μA	$V_{BB} \leq Vin \leq V_{CC}$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} +.3	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} \geq -1.6$mA, 1 TTL load
V_{OH}	Output High Voltage	2.4			V	$I_{OH} \leq 50\mu$A, 1 TTL load

POWER DISSIPATION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CCL}	V_{cc} Operating Current		8		mA	
I_{BBL}	V_{BB} Operating Current		8		mA	
I_{CCO}	V_{cc} Standby Current		0.8		mA	
I_{BBO}	V_{BB} Standby Current		0.8		mA	
P_{D0}	Standby Power Dissipation		8		mW	
P_{DI}	Operating Power Dissipation		80		mW	

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

(TG1 = TG2, Transmit Programmable Gain = 6dB; GSR = VFR−, Receive Programmable Gain = 0dB)

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response		±0.1		dB	Signal input of 0dBm0 f = 1.02KHz
DmW	Digital Milliwatt Response		±0.1		dB	f = 1.02KHz
$DmW_{\mu v}$	Digital Milliwatt Response VFR+, VFR−, μ-law		6.14		dBm	VFR+ single-ended output
DmW_{AV}	Digital Milliwatt Response VFR+, VFR−, A-law		6.17		dBm	R_L = 600Ω Receive input = 0mW sequence in CCITT G.711
$DMW_{\mu s}$	Digital Milliwatt Response at SAO, μ-law		3.70		dBVrms	No load; no sin x/x correction
DmW_{AS}	Digital Milliwatt Response at SAO, A-law		3.73		dBVrms	No load; no sin x/x correction
$OTLP_X$	Zero Transmission Level Point Transmit Channel (0dBm0)		.788 .785		Vrms Vrms	A-law μ-law

GAIN TRACKING

Reference level = 0dBm0 for μ-law, −10 dBm0 A-law at 1.02KHz, TG1 = TG2, GSR = VFR−, Transmit Programmable Gain = 6dB, Receive Programmable Gain = 0dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
GT_T	Transmit Gain Tracking Error Sinusoidal Input; μ or A-law		±.25 ±.50 ±1.2		dB dB dB	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0
GT_R	Receive Gain Tracking Error Sinusoidal Input; μ or A-law		±.25 ±.50 ±1.2		dB dB dB	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0 AT&T PUB43801 and CCITT G.712 — Method 2

ANALOG INTERFACE, RECEIVE PRIMARY AND SECONDARY CHANNELS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
R_{OR}	Output Resistance, VFR+ VFR−		1		Ω	
V_{OSR1}	Output Offset, VFR+ or VFR−, single ended		50		mV	Relative to GNDA
V_{OSR2}	Output Offset, VFR+ to VFR−, Differential		75		mV	
C_{LR}	Load Capacitance, VFR+, VFR−			100	pF	
V_{OR1}	Max Output Voltage Swing across R_L, VFR+, VFR−, single-ended connection	±3.2			Vp	$R_L \geq 300\Omega$
V_{OR2}	Max Differential Output Voltage Swing, VFR+, VFR−	±6.4			Vp	$R_L \geq 600\Omega$
P_{OR}	Differential Output Power, VFR+, VFR−			15.3	dBm	$R_L = 600\Omega$
R_{ORS}	Output Resistance, SAO		25		Ω	
V_{OSR}	Output Offset, SAO		50		mV	
C_{LRS}	Load Capacitance, SAO			20	pF	
R_{LRS}	Load Resistance, SAO	10			KΩ	
V_{ORS}	Output Voltage Swing SAO	±3.2			Vp	$R_L \geq 10K\Omega$

ANALOG INTERFACE, TRANSMIT PRIMARY AND SECONDARY CHANNELS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{BX}	Input Leakage Current, EBN1, EBN2, TG1		100		nA	−1.6V<VFX<1.6V
R_{IX1}	Input Resistance, VFX		500		KΩ	−1.6V<VFX<1.6V
R_{IX2}	Input Resistance, EBN1, EBN2, TG1		10		MΩ	±1.6V<VFX<1.6V
$CMRR_S$	Common Mode Rejection, SAI1, SAI2		40		dB	Differential SAI conversion
TGmax	Max Transmit Gain Adjust			20	dB	
V_{OTG}	Max Output Voltage Swing TG2	±1.6			v	$R_L \geq 10K\Omega$
C_{LX}	Load Capacitance, TG2			20	pF	
R_{LX}	Load Resistance, TG2	10			KΩ	

DISTORTION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
SD_X, SD_R	Signal to Distortion, μ or A-law Sinusoidal input; CCITT G.712 — Method 2 Half Channel	35 29 25			dB dB dB	0 to −30dBm0 −30 to −40dBm0 −40 to −45dBm0
DP_X, DP_R	Single Frequency Distortion Products In Band (2nd or 3rd Harmonic Half Channel)		−50	−47	dB	Input = 1.02kHz 0dBm0 AT&T Advisory #64 (3.8)
IMD_1	Intermodulation Distortion, End to End Measurement			−40	dBm0	CCITT G.712(7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−50	dBm0	CCITT G.712(7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−27	dBm0	CCITT G.712(6.1)
SIS	Spurious In Band Signals, End to End Measurement			−40	dBm0	CCITT G.712(9)
D_{AX}	Transmit Absolute Delay		180		μs	0dBm0, 1.02kHz Includes delay through A/D
D_{DX}	Transmit Differential Envelope Delay; Relative to minimum envelope delay (1.4kHz)		170 95 45 105		μs μs μs μs	f = 500–600 Hz f = 600–1000 Hz f = 1000–2600 Hz f = 2600–2800 Hz
D_{AR}	Receive Absolute Delay		125		μs	0dBm0, 1.02kHz Includes delay through D/A
D_{DR}	Receive Differential Envelope Delay; Relative to minimum envelope delay (300 Hz)		45 35 85 110		μs μs μs μs	f = 500–600 Hz f = 600–1000 Hz f = 1000–2600 Hz f = 2600–2800 Hz

NOISE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted		12		dBrnCO	Transmit Gain Adjust = 0dB
N_{XP1}	Transmit Noise, Psophometrically Weighted		−78		dBm0p	Transmit Gain Adjust = 0dB
N_{RC1}	Receive Noise, C-Message Weighted		10		dBrnCO	Unity Gain; Idle Code
N_{RP1}	Receive Noise, Psophometrically Weighted		−80		dBm0p	Unity Gain; Idle Code
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit or Receive Channel		−35		dB	Idle channel; 200mV P-P signal on supply DC to 50 KHz; Note 1.
$PSRR_2$	V_{BB} Power Supply Rejection Transmit or Receive Channel		−30		dB	Idle Channel; 200mV P-P signal on supply DC to 50 KHz; Note 1.

CROSSTALK

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
CT_{TR}	Crosstalk, Transmit Primary Voice to Receive Primary Voice		−75		dB	Input = 0dBm0, unity gain 1.02KHz; idle code on SLD voice and data bytes
CT_{RT}	Crosstalk, Receive Primary Voice to Transmit Primary Voice		−75		dB	0dBm0, 1.02 KHz signal at SLD receive voice byte; VFX = GNDA; secondary channels off
CT_{ST}	Crosstalk, Transmit Secondary Channels to Transmit Primary Voice		−70		dB	SAI = 0dBm0, 1.02 KHz; VFX = GNDA Idle code on SLD voice and data bytes
CT_{SR}	Crosstalk, Receive Secondary Channel to Receive Primary Voice		−70		dB	0dBm0, 1.02 KHz at SLD data byte VFX = SAI = GNDA

Note:
1. Measured at SLD Voice and Data bytes for transmit channel. Measured at $V_{FR}+$ for receive channel.

TRANSMIT VOICE FREQUENCY CHARACTERISTICS

TG1 = TG2, Transmit Programmable Gain = 6dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02kHz					0dBm0 Signal Input at VFX
	16.67Hz			−30	dB	
	50Hz			−25	dB	
	60Hz			−22	dB	
	200Hz	−1.8		−0.125	dB	
	300 to 3000Hz	−0.125		+0.125	dB	
	3300Hz	−0.35		+0.03	dB	
	3400Hz	−0.70		−0.10	dB	
	4000Hz			−14	dB	
	4600Hz and Above			−32	dB	
ΔG_{PX}	Programmable Gain		±.10		dB	freq. = 1.02kHz for all steps

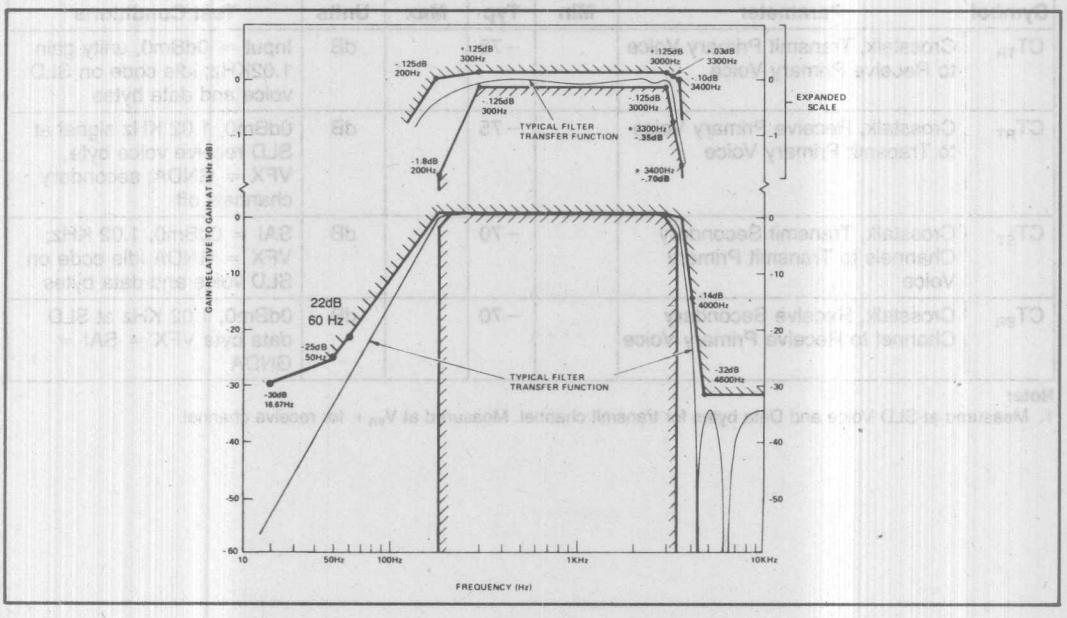
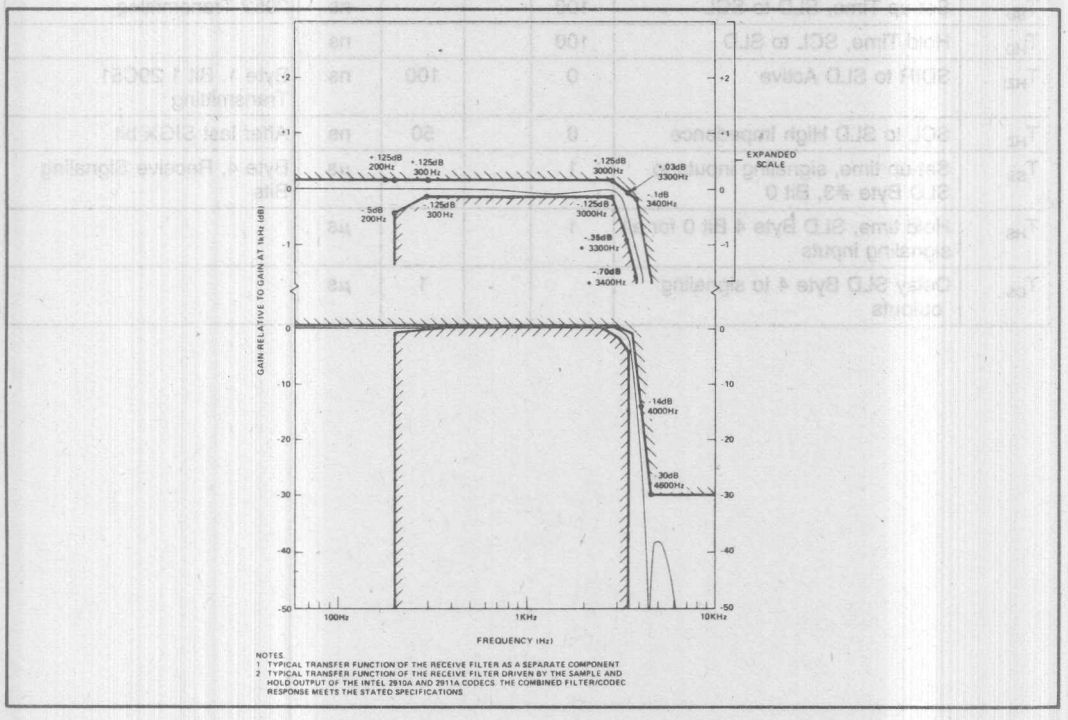


Figure 10. Transmit Voice Frequency Characteristics

RECEIVE VOICE FREQUENCY CHARACTERISTICS

GSR = VFR−, Receive Programmable Gain = 0dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RR}	Gain Relative to gain at 1.02kHz					0dBm0 input on SLD
	Below 200Hz			+0.125	dB	
	200Hz	−0.5		+0.125	dB	
	300 to 3000Hz	−0.125		+0.125	dB	
	3300Hz	−0.35		+0.03	dB	
	3400Hz	−0.70		−0.1	dB	
	4000Hz			−14	dB	
	4600Hz & Above			−30	dB	
ΔG_{PR}	Programmable Gain Accuracy		±.10		dB	f = 1.02kHz all steps

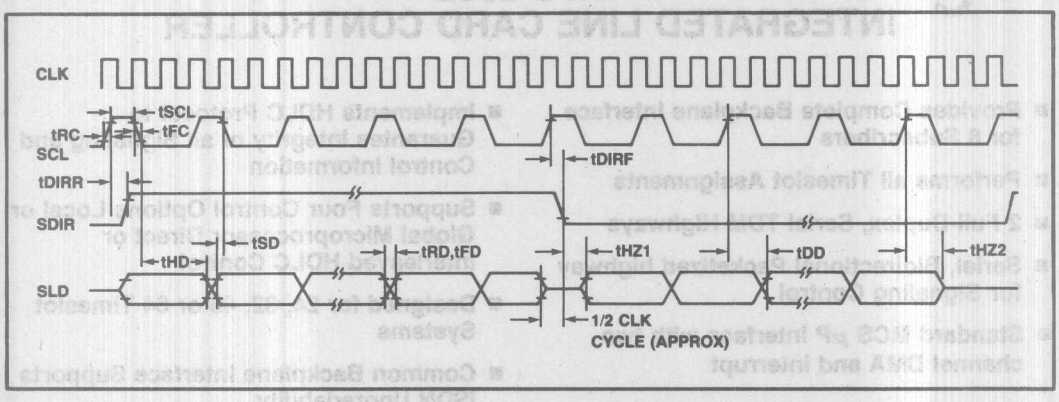


NOTES:
1. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER AS A SEPARATE COMPONENT.
2. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER DRIVEN BY THE SAMPLE AND HOLD OUTPUT OF THE INTEL 2910A AND 2911A CODECS. THE COMBINED FILTER/CODEC RESPONSE MEETS THE STATED SPECIFICATIONS.

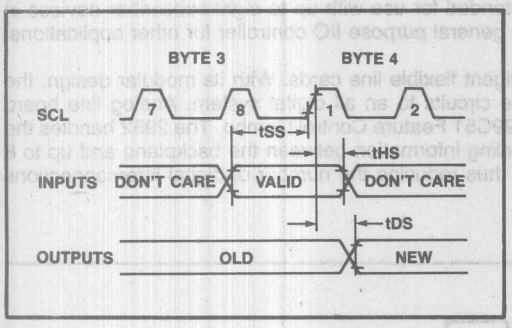
Figure 11. Receive Voice Frequency Characteristics

T_{SCL}	SCL Pulse Width	550		1075	ns	
T_{DC}	SCL Duty Cycle	28 45	33 50	38 55	% %	2952 CLK Clock = 1.544 or 1.536MHz 2952 CLK Clock ≥ 2.048MHz
T_{RC} T_{FC}	Rise, Fall Times, SCL			50	ns	
T_{RD} T_{FD}	Rise, Fall Times, SLD			50	ns	
T_{DIRR}	SCL to SDIR Delay	−100		100	ns	
T_{DIRF}	SCL to SDIR Delay	−100		+420	ns	
T_{DD}	SCL to SLD Delay	0		200	ns	29C51 Transmitting
T_{SD}	Set-up Time, SLD to SCL	100			ns	2952 Transmitting
T_{HD}	Hold Time, SCL to SLD	100			ns	
T_{HZI}	SDIR to SLD Active	0		100	ns	Byte 1, Bit 1 29C51 Transmitting
T_{HZ}	SCL to SLD High Impedence	0		50	ns	After last SIGX bit
T_{SS}	Set-up time, signaling inputs to SLD Byte #3, Bit 0	1			μs	Byte 4, Receive Signaling Bits
T_{HS}	Hold time, SLD Byte 4 Bit 0 for all signaling inputs	1			μs	
T_{DS}	Delay SLD Byte 4 to signaling outputs			1	μs	

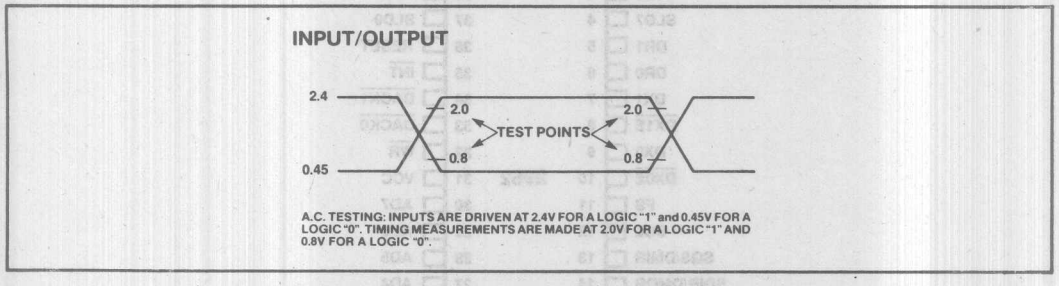
TIMING PARAMETERS (CLK = 1.544 MHz, 33% duty cycle)



SIGNALING TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM



iATC 2952
INTEGRATED LINE CARD CONTROLLER

- **Provides Complete Backplane Interface for 8 Subscribers**
- **Performs all Timeslot Assignments**
- **2 Full-Duplex, Serial TDM Highways**
- **Serial, Bidirectional Packetized highway for Signaling Control**
- **Standard MCS μP interface with two channel DMA and interrupt**
- **Implements HDLC Protocol to Guarantee Integrity of all Signaling and Control Information**
- **Supports Four Control Options Local or Global Microprocessor Direct or Interleaved HDLC Control**
- **Designed for 24, 32, 48 or 64 Timeslot Systems**
- **Common Backplane Interface Supports ISDN Upgradability**

The Intel iATC 2952 Line Card Controller (LCC) is a special purpose I/O controller optimized for use in all types of telecommunication switching systems. The 2952 is intended for use with up to eight subscriber devices in both analog and digital line circuits. It is also useful as a general purpose I/O controller for other applications.

The 2952 represents the continuation of a trend to intelligent flexible line cards. With its modular design, the 2952 provides a graceful upgrade path from analog line circuits to an all digital system. Analog line board density can be greatly increased using the LCC with the 29C51 Feature Control Combo. The 2952 handles the transfer of primary voice, data, feature control, and signaling information between the backplane and up to 8 29C51's. The 2952 emphasizes highly serial interfaces, thus reducing the number of digital interconnections both to the subscriber device and to the backplane.

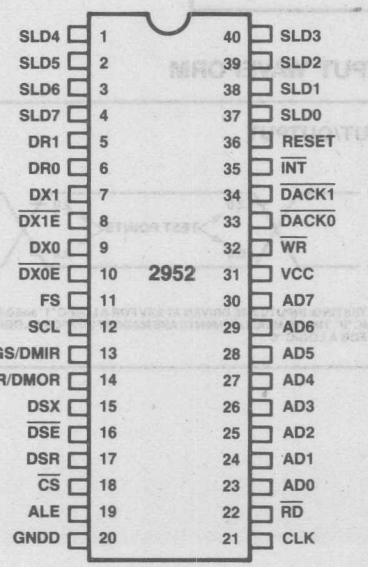


Figure 1. Pin Configuration

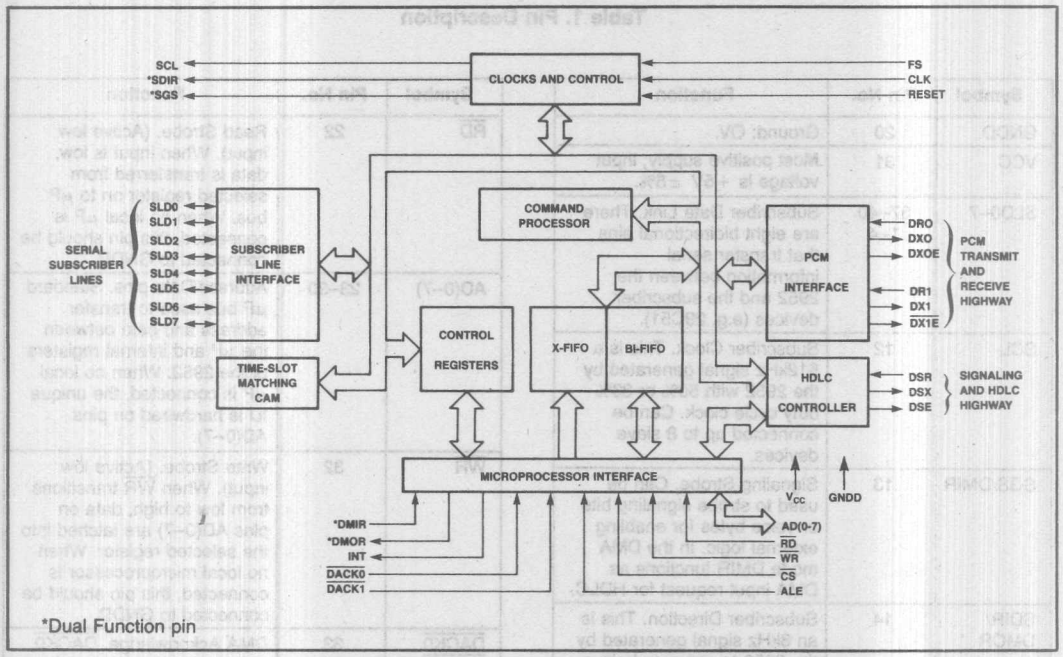


Figure 2. 2952 Block Diagram

Table 1. Pin Description

Symbol	Pin No.	Function
GNDD	20	Ground: OV.
VCC	31	Most positive supply; input voltage is +5V ±5%.
SLD0–7	37–40 1–4	Subscriber Data Link. There are eight bidirectional pins that transfer serial information between the 2952 and the subscriber devices (e.g. 29C51).
SCL	12	Subscriber Clock. This is a 512kHz signal generated by the 2952 with 50% or 33% duty cycle clock. Can be connected up to 8 slave devices.
SGS/DMIR	13	Signaling Strobe. Can be used to strobe signaling bits or voice bytes for enabling external logic. In the DMA mode DMIR functions as DMA input request for HDLC.
SDIR/ DMOR	14	Subscriber Direction. This is an 8kHz signal generated by the 2952 to serve as both a direction indicator and a slave frame sync. When high, the SLD bus becomes an output and data is transferred from the 2952 to the slave. When low, the output buffer on the slave SLD pin is enabled and data is transferred from the slave to the 2952. In the DMA mode, DMOR functions as DMA output request for HDLC.
$\overline{CS}$	18	Chip Select. Enables $\overline{RD}$ or $\overline{WR}$. A low level at this input allows the 2952 to accept commands or data from a microprocessor within a write cycle, or to transmit data during a read cycle. When no local uP is connected this pin should be connected to GNDD.
ALE	19	Address Latch Enable. (Active high input). On falling edge of this input signal, data on AD(0–7) is latched into the selected register. When no local microprocessor is connected, this pin should be connected to GNDD.

Symbol	Pin No.	Function
$\overline{RD}$	22	Read Strobe. (Active low input). When input is low, data is transferred from selected register on to μP bus. When no local μP is connected, this pin should be connected to GNDD.
AD(0–7)	23–30	Address/Data pins. Standard μP bus used to transfer address and data between the μP and internal registers of the 2952. When no local μP is connected, the unique ID is hardwired on pins AD(0–7).
$\overline{WR}$	32	Write Strobe. (Active low input). When $\overline{WR}$ transitions from low to high, data on pins AD(0–7) are latched into the selected register. When no local microprocessor is connected, this pin should be connected to GNDD.
$\overline{DACK0}$ $\overline{DACK1}$	33 34	DMA Acknowledge. $\overline{DACK0}$ is used to acknowledge the DMA output, and $\overline{DACK1}$ is used for DMA input. When no local microprocessor is connected, these pins are used to hardwire mode information.
$\overline{INT}$	35	Interrupt Request. A standard microprocessor interrupt, with active low output.
DR1	5	Receive PCM Highway 1. Serial words are received on PCM highway 1 at this interface.
DR0	6	Receive PCM Highway 0. Serial words are received on PCM highway 0 at this interface.
DX1	7	Transmit PCM Highway 1. Serial words are transmitted onto PCM highway 1 at this interface.
$\overline{DX1E}$	8	Transmit PCM Highway 1 Enable. Used to enable external tristate buffers to drive signals onto the PCM highway. The signal goes low while the 2952 is transmitting onto PCM highway 1.

Table 1. Pin Description

Symbol	Pin No.	Function
DX0	9	Transmit PCM Highway 0. Serial words are transmitted onto PCM highway 0 at this interface.
$\overline{DX0E}$	10	Transmit PCM Highway 0 Enable. Used to enable external tristate buffers to drive signals onto the PCM highway. The signal goes low while the 2952 is transmitting onto PCM highway 0.
DSX	15	Transmit Signaling Highway. Serial signaling and control data is transmitted on this dedicated HDLC highway.
$\overline{DSE}$	16	Transmit Signaling Highway Enable. Used to enable external tristate buffers to drive signals onto the transmit signaling highway. The signal goes low while the 2952 is transmitting an HDLC packet onto DSX.
DSR	17	Receive Signaling Highway. Serial signaling and control data is received on this dedicated HDLC highway.
FS	11	Frame Synchronization System sync pulse indicating beginning of a 125 μsec frame.
CLK	21	Master Clock. System input clock provides basic timing for the 2952 and is synchronous to the PCM clock. The clock rate determines the number of timeslots on the transmit and receive PCM highways, ranging from 24, 32, 48 or 64 per frame.
RESET	36	Reset. (Active high input). When high, 2952 internal circuitry is reset. The minimum reset pulse must be 16 complete CLK clock cycles wide.

FUNCTIONAL DESCRIPTION

The 2952 is a highly integrated line card controller which concentrates and multiplexes all digital information that passes between a line card and the next switching or control level in a digital telecommunications system. It controls time switching functions between the individual subscriber line devices and the system backplane Time Division Multiplexed (TDM) highways. In addition, it manages the transfer of all signaling and control messages, either to an optional local microprocessor or to a central control processor. The 2952 implements all protocol control functions using the HDLC format for all information transmitted between the line card and the central processor.

EXTERNAL INTERFACE

The 2952 LCC supports interfaces for the subscriber line devices, an optional local microprocessor, and the backplane PCM and HDLC highways. Each is described briefly below.

Subscriber Line Interface

The LCC provides 8 serial, bidirectional ports for the digital transmission of voice, data, control, and signaling information to and from the subscriber. These leads, SLD0–SLD7, can be used to interface to both analog and digital line card subscribers (See Figure 3).

The Slave Clock SCL, is a fixed 512 kHz signal output used to transfer all signals between the subscriber device and the 2952. Data is received and transmitted upon the rising edge of SCL.

Data transmission direction is controlled by the Slave Direction clock, SDIR. This 8 kHz signal divides the frame transfer into transmit and receive halves referenced to the subscriber as shown in Figure 3. When SDIR is high, (RCV half-cycle), information is transmitted from the 2952 to the subscriber in four bytes consisting of voice, data, feature control, and signaling information. In the second half (XMIT-half cycle), the subscriber circuit sends four bytes of XMIT data back to the 2952.

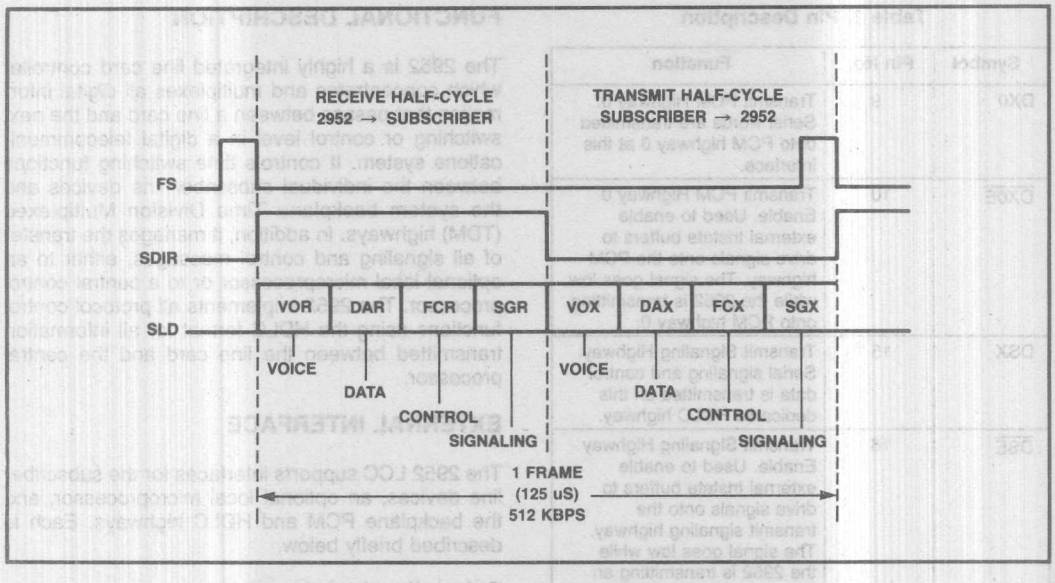


Figure 3. SLD Interface

Backplane Interface

The LCC supports dual TDM voice/data highways as well as a separate high speed serial highway for signaling and control information. This information is packetized and protected in HDLC format for transmission to a central processor.

The system clock (CLK) provides data rate transfers for both the TDM and HDLC links. The 2952 can operate in 24, 48, 32 or 64 timeslots systems. Any subscriber has access to any timeslot on either TDM highway. The 2952 allows the flexibility of programmable rising or falling edge latching of data onto the highways. Additionally, PCM highway delays can be compensated for by programming a phase shift in both transmit and receive timeslots as referenced to the frame synchronization pulse. The starting point of the bytes can be shifted up to 7 CLK clock cycles for both transmit and receive directions in half clock increments.

Microprocessor Interface

The microprocessor interface provides a communication path for a local μP and the backplane and/or slave devices. The 2952 is designed to operate with standard Intel 8-bit parallel microprocessors, such as the MCS-48, MCS-51, MCS-85, and MCS-86 families. Interrupt capability, direct-memory-access request and acknowledge signals and a full feature multiplexed address data bus are incorporated into this interface.

Alternatively, the 2952 can operate in a stand alone mode on the line card in systems using a more centralized processing architecture. In this mode, the individual line board address and initialization information is hardwired onto the microprocessor interface pins.

2952 BASE ARCHITECTURE

The 2952 can be partitioned into three functional blocks, according to the type of data transfers that each provides. The synchronous portion comprises the subscriber and PCM highway interfaces. Included in this section is also the Master Timing Unit, a CAM (Content Addressable Memory) for timeslot matching, a MODE register to configure the 2952 and for the determination of the type of HDLC data exchange, and the internal bus for a communication link between the various interfaces and registers. The PCM Interface Unit and the Subscriber Interface Unit with Last Look logic are also grouped into this segment. The Last Look logic monitors the status of signaling information received from each subscriber every frame. Any change of status is reported to the local μP or to the LCC bus control unit.

The asynchronous portion includes the local microprocessor interface and the serial HDLC signaling and control interface. The HDLC controller is compatible with ISO/CCITT recommendation X.25, and is designed for either point-to-multipoint configurations as a primary station, or in point-to-point as a secondary station. Each 2952 is accessed through

an 8-bit address, allowing up to 255 secondaries to be addressed on one HDLC serial line. The logic level of the HDLC implementation and the distribution and compilation of the data packages are handled in a separate command unit contained in this portion.

The synchronous and asynchronous portions are linked to one another by a set of buffers and a control unit for the LCC internal bus. Two 16-byte by 8-bit FIFO's are used for intermediate storage of messages. An X-FIFO, or Transmit FIFO buffers data packages for transmission to the central processor through the HDLC interface. The type of data loaded is either from the Last Look logic or from the μP in package form with direct addressing to the 2952. The Bi-FIFO, or bidirectional FIFO, is used for data exchange between the central controller (via the HDLC interface), the local microprocessor (via the μP bus), and the LCC (via the LCC bus).

MODES OF OPERATION

The 2952 may operate in either a primary or secondary command mode within a single system. When instructed as a primary station, a local microprocessor must be used to instruct the 2952 and to generate control messages for other stations. This mode is used primarily by unit or group controllers to command secondary 2952's. When in the secondary mode, the 2952 executes received HDLC commands from the group controller. Additionally, a transparent command mode may be configured in which all HDLC messages received from the backplane are passed directly to the local microprocessor. This allows a secondary 2952 to execute user defined protocol and commands.

The 2952 can operate in one of two HDLC communication modes — dedicated HDLC or interleaved HDLC. In the dedicated configuration, HDLC messages are received on DSR and are transmitted on DSX. The interleaved mode reserves up to two timeslots per frame for transmission of signaling and control messages on the PCM highways. The HDLC packets are disassembled and interleaved into programmed timeslots on either of the two highways. Alternatively, the microprocessor can communicate directly to the central controller via a direct connection, bypassing the 2952 HDLC interface completely.

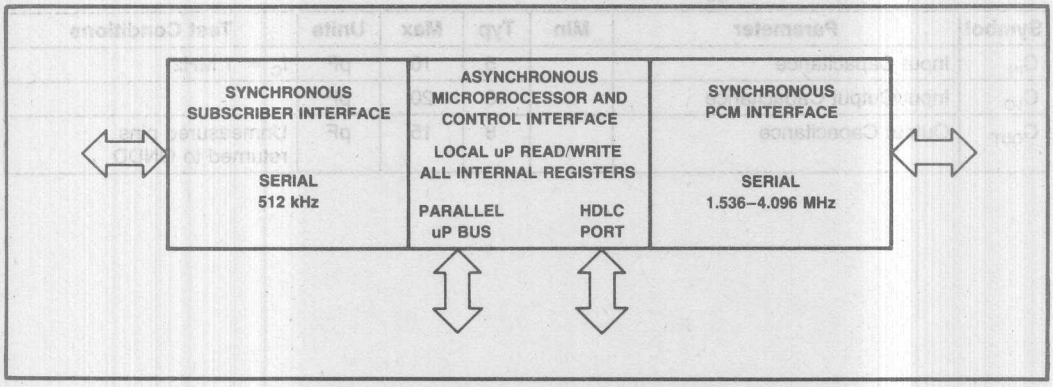


Figure 4. Architectural Diagram

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias −10°C to +80°C
Storage Temperature −65°c to 125°C
All Input and Output Voltages
with respect to GNDD −0.3V to +7V
Total Power Dissipation 1.5W

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%; GNDD = 0V
Typical values are for T_A = 25°C and nominal power supply value

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Leakage Current	−10		+10	μA	GND ≤ V_{IN} ≤ V_{CC}
I_{OL}	Output Leakage Current	−10		+10	μA	GND ≤ V_{OUT} ≤ V_{CC}
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V		
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = +1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		85	120	mA	V_{CC} = 5V
P_{D1}	Operating Power Dissipation		425		mW	

CAPACITANCE (T_A = 25°C; V_{CC} = GNDD, 0V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_{IN}	Input Capacitance		5	10	pF	f_C = 1 MHz
$C_{I/O}$	Input/Output Capacitance		10	20	pF	
C_{OUT}	Output Capacitance		8	15	pF	Unmeasured pins returned to GNDD

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ± 5%, GNDD = 0V)

SLD Interface Timing

Symbol	Parameter	Min	Max	Units
CLK	System Backplane Clock Frequency	1.536	4.096	MHz
	CLK Duty Cycle	45	55	%
t_{PFS}	Frame Synchronization Pulse Period	125		μS
t_{FS}	Frame Synchronization Pulse Width	60	t_{CLK}	ns
t_{dFS}	Pulse Delay to CLK	10		ns
t_{SFS}	Set-Up Time to CLK	50		ns
t_{rf}	CLKRise, Fall Times		10	ns
SCL	Slave Clock SCL Frequency	512	512	kHz
t_{dSCL}	SCL Delay Time From CLK	100	165	ns
SDIR	Slave Direction SDIR Frequency	8	8	kHz
t_{dDIR}	SDIR Delay Time to CLK	120	190	ns
t_{dSLD}	SLD Data Delay	160	300	ns
t_{DER}	Data Enable Receive	100	180	ns
t_{DDR}	Data Disable Receive	100	180	ns
t_{DEX}	Data Enable Transmit	0		ns
t_{DAX}	Data Hold Transmit	0		ns
t_{DSX}	Data Set-Up Transmit	$\frac{1}{2\ CLK} + 200$		ns
t_{DSIG}	Signaling Strobe Delay	110	160	ns

A.C. CHARACTERISTICS
(T_A = 25°C, V_{CC} = GNDD = 0V)

MICROPROCESSOR INTERFACE

READ CYCLE

Symbol	Parameter	Min	Max	Units
t_{AL}	Address Set-Up to ALE	30		ns
t_{LA}	Address Hold After ALE	20		ns
t_{AA}	ALE Pulse Width	60		ns
t_{RD}	Data Delay From $\overline{RD}$		150	ns
t_{DF}	Data Float After $\overline{RD}$		25	ns
t_{RR}	$\overline{RD}$ Pulse Width	150	10^7	ns
t_{RI}	$\overline{RD}$ control interval[1]	$2 \times \frac{1}{.CLK}$		ns
t_{RI}	$\overline{RD}$ control interval[2]	100		ns

WRITE CYCLE

Symbol	Parameter	Min	Max	Units
t_{DW}	Data Set-Up to $\overline{WR}$	50		ns
t_{WD}	Data Hold After $\overline{WR}$	25		ns
t_{WW}	$\overline{WR}$ Pluse Width	100		ns
t_{WI}	$\overline{WR}$ control interval[1]	$2 \times \frac{1}{.CLK}$		ns
t_{WI}	$\overline{WR}$ control interval[2]	50		ns

NOTES:
1. Read or Write of BI FIFO and X FIFO.
2. Read or Write of all other registers.

DMA READ

Symbol	Parameter	Min	Max	Units
t_{DMA}	DMA Read Time		$7 \times \frac{1}{.CLK}$	ns
t_{OH}	DMOR Hold Time		75	ns
t_{AR}	Address Stable before $\overline{RD}$	0		ns
t_{RD}	Data Delay from $\overline{RD}$		150	ns
t_{DH}	Data Hold after $\overline{RD}$	20		ns
t_{RA}	Address Hold after $\overline{RD}$	0		ns
t_{RR}	$\overline{RD}$ Pulse Width	150	10^4	ns

DMA WRITE

Symbol	Parameter	Min	Max	Units
t_{DMA}	DMA Write Time		$7 \times \frac{1}{.CLK}$	ns
t_{IH}	DMIR Hold Time		80	ns
t_{AW}	Address Stable before $\overline{WR}$	0		ns
t_{WA}	Address Hold after $\overline{WR}$	0		ns
t_{DW}	Data Set-Up to $\overline{WR}$	30		ns
t_{WD}	Data Hold after $\overline{WR}$	25		ns
t_{WW}	$\overline{WR}$ Pulse Width	100		ns

System Backplane Timing Parameters

PCM INTERFACE — RECEIVE TIMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{DSRR}	Receive Data Set-Up DCR = 0[1]	40		ns	60ns for Interleaved Mode
t_{DHRR}	Receive Data Hold DCR = 0[1]	10		ns	
t_{DSRF}	Receive Data Set-Up DCR = 1[2]	20		ns	
t_{DHRF}	Receive Data Hold DCR = 1[2]	40		ns	

PCM INTERFACE — TRANSMIT TIMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{DZXR}	Data Enable DCX = 0	80	160	ns	C_L = 200pF
t_{DHXR}	Data Hold Time DCX = 0	45	160	ns	C_L = 200pF
t_{DZXF}	Data Enable DCX = 1	40	100	ns	C_L = 200pF
t_{DHXF}	Data Hold Time DCX = 1	40	100	ns	C_L = 200pF
t_{HZX}	Data Float After CLK TS	35	80	ns	C_L = 150pF
t_{SONR}	Timeslot x to enable DCX = 0	70	130	ns	C_L = 150pF
t_{SONF}	Timeslot x to enable DCX = 1	40	100	ns	C_L = 150pF
t_{SOFF}	Timeslot x to disable	40	100	ns	C_L = 150pF

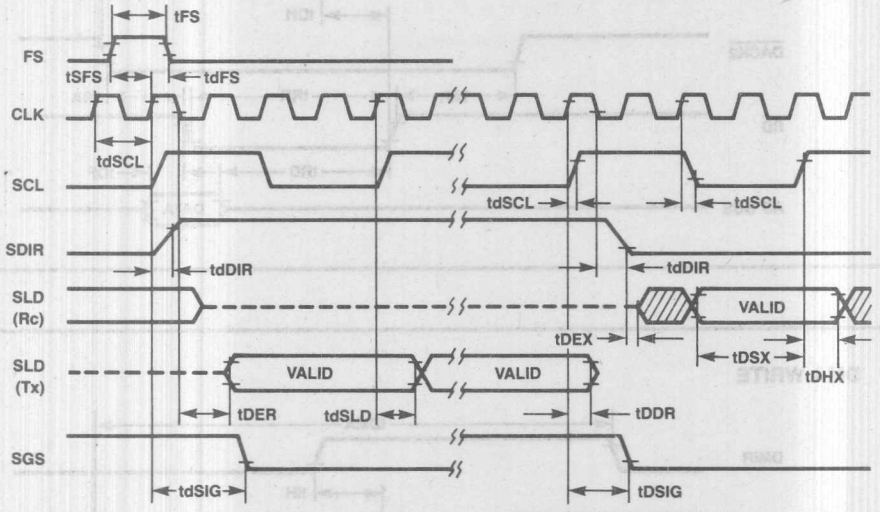
HDLC INTERFACE TIMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{DS}	Receive Data Set Up	40		ns	
t_{DM}	Receive Data Hold	10		ns	
t_{TD}	Transmit Data Delay	40	100	ns	C_L = 200pF
t_{HZX}	Data Float on TS Exit	35	80	ns	C_L = 200pF
t_{SON}	Timeslot X to enable	40	95	ns	C_L = 150pF
t_{SOFF}	Timeslot X to enable	35	90	ns	C_L = 150pF

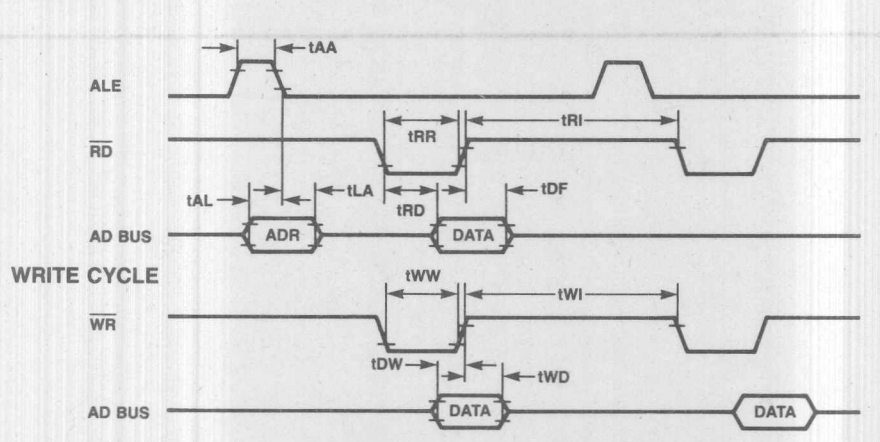
NOTE:
1. DCR = 0 data latched on rising edge of CLK.
2. DCR = 1 data latched on falling edge of CLK.

WAVEFORMS

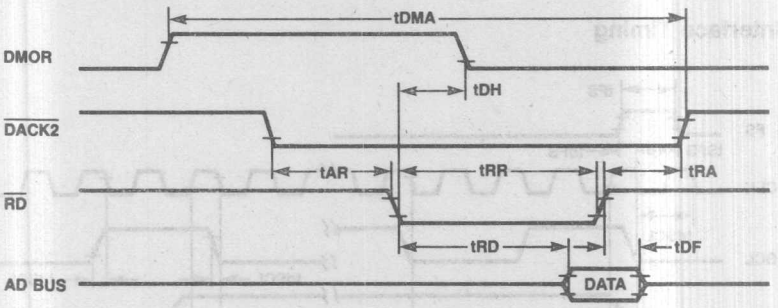
SLD Interface Timing



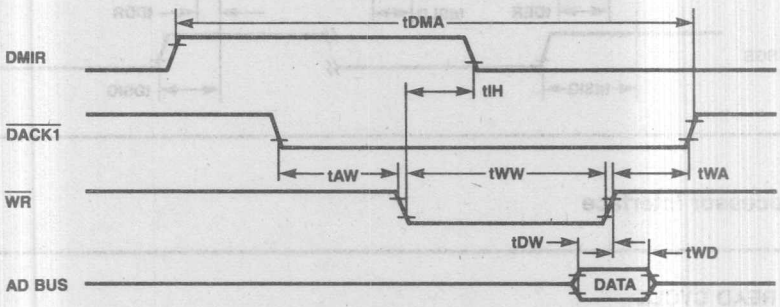
Microprocessor Interface



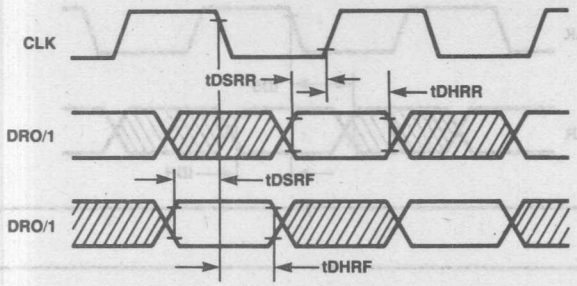
DMA READ



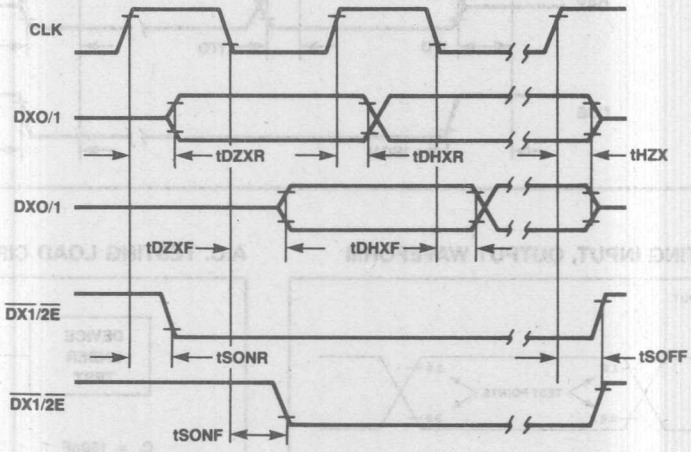
DMA WRITE



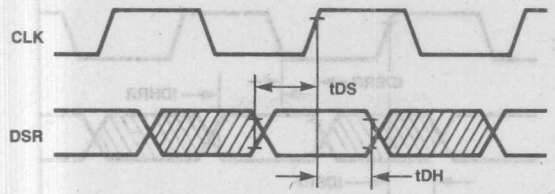
PCM INTERFACE RECEIVE TIMING



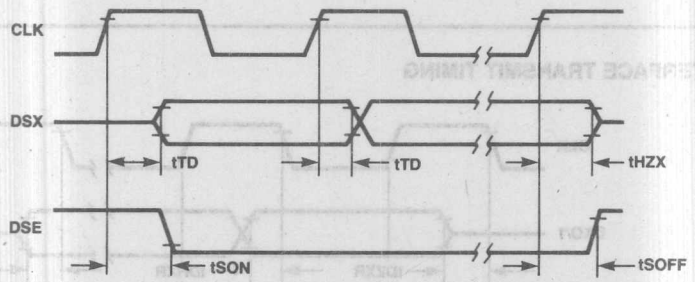
PCM INTERFACE TRANSMIT TIMING



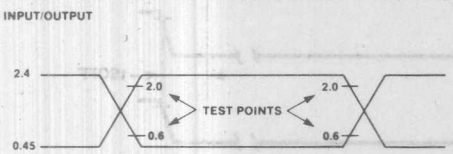
HDLC INTERFACE RECEIVE TIMING



HDLC INTERFACE TRANSMIT TIMING

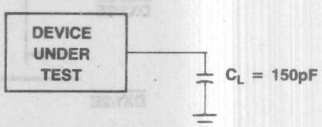


A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.6V FOR A LOGIC "0".

A.C. TESTING LOAD CIRCUIT



C_L = 150pF
C_L INCLUDES JIG CAPACITANCE

Two programmable ICs enhance line-card functionality

Besides handling subscriber-line interface tasks, this chip pair takes over such responsibilities as time-slot assignment

by Fred H. Cherrick and Bhupendra K. Ahuja, *Intel Corp., Chandler, Ariz.*

☐ In a major step toward the fully integrated telecommunications line card, two complementary-MOS integrated circuits will make possible computer control of the card's functions. The iATC 29C51 provides coding and decoding between subscriber-line and pulse-code–modulated signals, filtering, and hybrid balancing—all on a single chip. As well as being programmable, it includes a number of capabilities ordinarily requiring much additional discrete circuitry. Complementing this IC is an advanced line-card controller, the iATC 29C52, which gives the card extra intelligence to manage the increased number of lines and the additional functions made available by a higher level of integration.

These two chips are the first of a family aimed at realizing the concept of an integrated-services digital network, or ISDN (see "Making phone calls digital end to end: the ISDN," opposite). Their programmability brings important control functions down to the line-card level from the central switching office. Programmability also makes possible such new features as automated testing of the line-card functions.

In today's analog network, the Borscht (for battery feed, overvoltage protection, ring generation, supervision, codec, hybrid impedance balancing, and testing) functions (Fig. 1) make up the requirements for a line circuit in a digital switch. This circuit has generally been built with discrete devices, transformers, and in some cases, test relays. However, the obvious benefits of integration have already produced single-chip codec-filters.

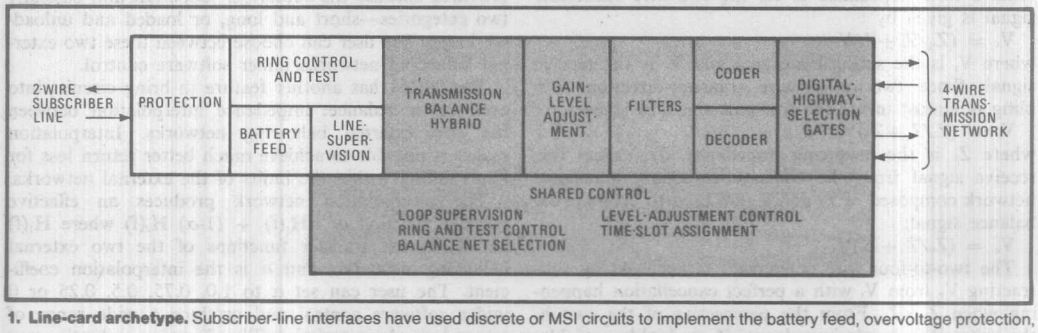
Recent developments have shown that the BOR functions of battery feed, overvoltage protection, and ringing can be effectively integrated in bipolar technology. Also, the functions of supervision, hybrid impedance balancing, and testing are being implemented as single C-MOS chips.

The 29C51 (Fig. 2) goes beyond these chips by including all the features available in standard codec-filter and impedance-balancing chips, plus extra capabilities aimed at improving system efficiency. The extra capabilities can be categorized as feature control, a secondary voice or data channel, and signaling. Feature control refers to the ability of the 29C51 to be managed by commands originating in system software and is achieved by making key functions user-programmable, such as gain adjustments, loop-back testing, and impedance balancing. The secondary channel can be used for many purposes, including conferencing and telemetry. Signaling is the routing of status information concerning individual subscriber lines, such as hook condition, dialing, and ring detection.

The need for impedance balancing

Because of the high voltages on the two-wire subscriber line and the requirement for separate receive and transmit digital channels, transformers are used to convert signals to the four-wire transmission level. But because mismatched impedances can affect transformer coupling, a hybrid impedance-balancing circuit is needed between two-wire analog subscriber loops in a four-wire transmission system where separate wire pairs are assigned for the transmit and receive directions.

In a two-to-four-wire system, there is almost unity



1. Line-card archetype. Subscriber-line interfaces have used discrete or MSI circuits to implement the battery feed, overvoltage protection, ring generation, supervision, codec-filter, hybrid balancing, and testing (the Borscht functions). Two VLSI chips perform the tasks as highlighted.

Making phone calls digital end to end: the ISDN

The advent of large-scale integrated circuits has sparked an explosion in distributed data processing. Although less evident to the user, this development is also causing major changes in telecommunications networks. For distributed computing to continue spreading, enhanced telecommunications capabilities must be developed in the form of a true end-to-end digital communications network. Work on a unified definition of such a network is under way in committees of the International Telecommunications Union and the 1980s are expected to be the beginning of ISDN—the integrated-services digital network.

Although the ISDN concept is not set in concrete, several requirements for handling voice and data in public and private networks are becoming evident. As is true of most business and consumer markets, costs determine the growth rate of enhanced services, so LSI technology will play an important role in the development of a practical digital network.

Also, because an enormous analog telecommunications network is already installed, it is likely that ISDN will evolve rather than develop rapidly, even if a standard is developed. In the U. S., American Telephone & Telegraph Co. has proposed a plan to provide service with alternate voice and data transmission, capable of 56-kilobit-per-second bidirectional data rates over a single subscriber line. AT&T has also proposed an analog-based simultaneous voice and data service with a 4.8-kb/s data rate. However, many European telecommunications authorities want to implement a fully digital 144-kb/s service consisting of two 64-kb/s voice or data channels and a 16-kb/s signaling or voice-and-data channel.

Other considerations of ISDN involve control structure, interchangeability of terminal equipment, and system signaling. In this environment, the components must be designed to support multiple capabilities when possible. Currently, nearly all public switching is analog, with digital transmission used to increase channel efficiency. The transmission of data requires special routing and handling in this network impeding the full benefits of a simultaneous voice-and-data ISDN. As the network becomes increasingly digital, including subscriber-line local loops, the ISDN becomes less difficult to switch and maintain and its benefits less costly. To hasten this conversion, LSI component solutions must be flexible enough to provide telecommunication services for both network architectures.

The iATC family is this type of solution. The diagram shows how such a conversion of analog to digital subscriber lines will be accommodated by the addition of future iATC components aimed at providing digital formatting in the phone terminal equipment.

coupling between the two wires in the transmiting direction and the two on the receiving side. However, there can be undesirable coupling of signals from the receiving to the transmitting direction. This coupling results in an echo to the calling party if the loop impedance is significant enough to unbalance the two-to-four-wire hybrid. The intent of the balancing is to improve the return loss from the receive to transmit direction.

The 29C51 includes the two-to-four-wire conversion with software-programmable balancing so that return loss can be optimized for various subscriber-line conditions. This programmability is better understood by looking at the specific conditions needed for a subscriber line to be balanceed and have a low return loss.

If the receive side of a hybrid balancing network has an output impedance of Z_o, and the two-wire side presents a load impedance of Z_l, the two-wire subscriber signal is given by :

$$V_s = (Z_{fi}/Z_o + Z_l)V_r$$

where V_s is the subscriber signal and V_r is the receive signal. Since two-to-four-wire transmit-direction coupling is almost unity, the transmit signal is given by:

$$V_t = (Z_l/Z_o + Z_b)V_r$$

where Z_b is the balancing impedance. To cancel this receive signal from the transmit direction, a balance network composed of Z_o and Z_b are used to produce the balance signal:

$$V_b = (Z_o/Z_o + Z_b)V_r$$

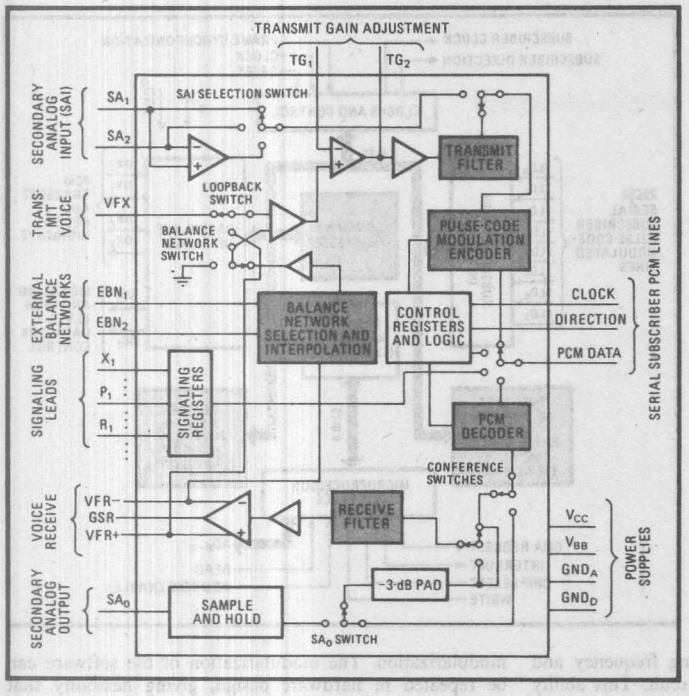
The two-to-four-wire conversion is achieved by subtracting V_b from V_t with a perfect cancellation happening when $Z_b = Z_l$. From the perspective of the switch, the subscriber loop's impedance, Z_l, is highly variable, due to such factors as different loop lengths and wire guages. However, because it is impractical to make balance impedances equally variable, hybrid balance can only be approximated by a discrete network, Z_b and Z_o, to achieve an allowable system return loss.

The 29C51 provides the three most commonly used test balancing networks: some systems may also use them as the regular balancing networks. These three common networks have been integrated in a switched-capacitor–filter configuration, and their output is subtracted from the transmit signal. The user may choose any of them under software control.

To meet varying requirements for two-to-four-wire conversion, two pins have been provided with which a user can also connect custom balance networks and still perform the signal subtraction on chip. These pins are provided because the subscriber loops fall into basically two categories—short and long, or loaded and unloaded, loops. The user can choose between these two external balancing networks under software control.

The 29C51 has another feature to bring circuits into even better balance: impedance interpolation between the two external balancing networks. Interpolation makes it possible to achieve much better return loss for loops falling within the limits of the external networks.

The interpolation network produces an effective transfer function of $\alpha H_1(f) + (1-\alpha) H_2(f)$ where $H_1(f)$ and $H_2(f)$ are transfer functions of the two external balancing networks, and α is the interpolation coefficient. The user can set α to 1.0, 0.75, 0.5, 0.25 or 0 under software control and produce a wide range of return-loss characteristics (Fig. 3) using only the two



networks to serve the extremities of loop conditions.

Gain levels for receive and transmit functions in the 29C51 can be adjusted in less than a millisecond and are dynamically controllable within software constraints. Programmable analog and digital loop-back modes are designed to automate as much of the test function as possible. In analog loop-back, a PCM byte can be decoded into analog form and encoded into digital form to provide a response byte that the system can compare with the original transmission. In digital loop-back, an analog input to the primary or secondary line can be encoded, transferred to the receive input, and decoded to return the signal in the primary analog channel. Both features are useful for a variety of test functions associated with line quality and balancing.

Along with its primary voice channel, the 29C51 has a secondary channel for a simultaneous information signal. This feature may be used in many different applications, such as telemetry, teleconferencing, remote loop testing, and control. The channel actually provides two secondary analog inputs (SAI), which can be encoded in a differential or single-ended mode as an 8-bit μ-law or A-law companded PCM word at an 8-kilohertz sampling rate. On the receive side, a secondary analog output (SAO) is provided, which is the decoded value of the received 8-bit PCM control data.

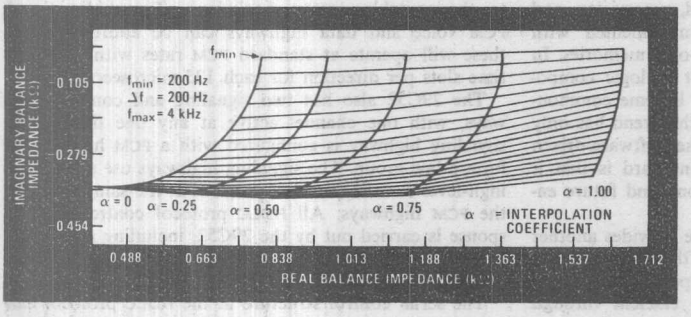
Applications such as reading power and water meters or other narrow-bandwidth analog signals can be sampled at 8 kHz by the 29C51 encoder and the digitized words sent to a central processing location. Similarly, the SAO can be used to control electrical appliances by sending different PCM words for on or off conditions to the 29C51. One such application of this feature is in controlling power-load peaking for utilities.

Secondary-channel uses

The secondary channel also can provide conference calling. In this mode, it is instructed to add a second analog signal following the decoding of the primary voice channel so these signals can then be filtered together. This valuable conferencing tool can be expanded through iterations of the process in different line circuits and in specific conferencing circuits.

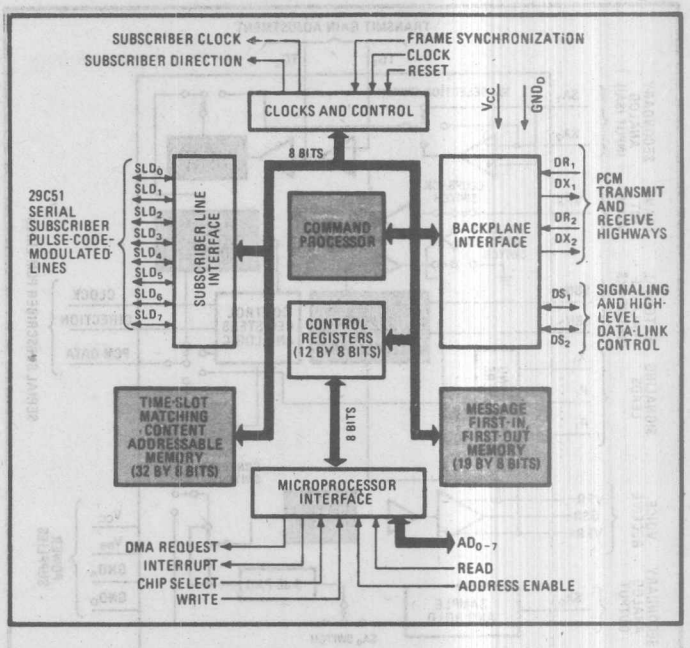
However, no input band-limiting filters or output-smoothing filters are present on the 29C51 for this secondary channel. Therefore, either the user must provide this filtering off chip or else limit the applications of the secondary channel to carrying signals having less than a 4-kHz bandwidth.

The secondary channel can also be used in remote loop testing where the battery voltage or the loop current is a dc variable to be monitored



2. Software-switched functions. To set programmable functions such as attenuation, hybrid impedance balancing, loop-back testing, and primary or secondary channel selection, users of the iATC 29C51 send control commands to on-chip registers over a serial port. Gain and impedance balance values may also be established externally.

3. Interpolated impedance range. The 29C51 has an impedance-balancing feature with which a wide variety of values can be obtained by interpolating between fixed minimums and maximums set externally. Values of α equal to 1 and 0 yield the external balance values; fractional α values produce a better balance over the frequency spectrum.



4. Complex control made simple. Connection of eight subscriber lines to pulse-code-modulated transmission highways and their signaling channels is made easy in the iATC 29C52 line-card controller by compiling HDLC commands on chip. A content-addressable memory reduces control overhead by assigning time slots automatically.

as a secondary analog input. The encoded values of the voltage or current can be processed to determine if a loop requires a voltage boost. The desired values can be sent as a PCM word to the 29C51 on the secondary channel, and the decoded value from the SAO can be a control input to the line card to allow adjustment of the battery voltage.

The secondary channel can also detect the on- or off-hook signal. The loop current is a good monitor of this signal, which can be encoded at a SAI, thus simplifying the signaling overhead of a subscriber-line interface circuit. Similarly, the ringing tone can be sent as digitized PCM words, which when decoded at the SAO can be used to control the ringing frequency and amplitude in a particular subscriber circuit. This ability can save considerable amounts of discrete circuitry most line cards include to perform the signaling functions: identifying and controlling subscriber-loop conditions such as ringing, and on- or off-hook.

The 29C51 uses a simple communications link between its ports and a line-card controller. This configuration reduces the digital interface requirements for synchronous receive and transmit operation from 13 connections to the digital backplane for timing and data in current codec-filters to three pins in the 29C51—the bidirectional data lead, a clock, and the data direction signal.

The chip also is equipped with a set of dedicated signaling pins to link with line hardware that performs the BOR functions. The pins will work with advanced single-chip BOR circuits such as one described by Harris Corp. at the International Solid State Circuits Conference last month. With such a chip, the subscriber-line circuitry is reduced to two ICs.

Until recently, subscriber-line control, supervision, and PCM-interface functions have been implemented with standard logic and programmable read-only memories. In private branch exchanges, replacement of logic components by a microprocessor has already become commonplace, while in central-office switches, this trend has only just begun. A major advantage of the software-driven structure of a microprocessor-based line card is that it lends itself to advanced analog telephony and future enhanced services.

The presence of line-card intelligence provides another opportunity for distributed control in the switching system. Software development, a major portion of system design cost, can also be made more efficient through modularization. The modularization of the software can be repeated in hardware design, giving flexibility that promotes cost-effective modules with different levels of voice or voice-and-data service.

With much of the control function integrated and an on-chip high-level–protocol interface, the 29C52 (Fig. 4) represents the continuation of the trend to flexible, intelligent line cards. As a dedicated large-scale integrated line-card controller, it provides distributed control by exploiting the capabilities of the 29C51.

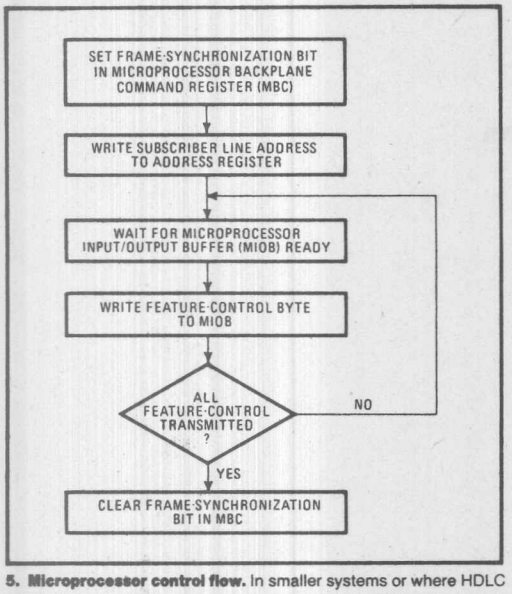
Exchanging signals

The controller IC has a subscriber-line interface operating synchronously with up to eight 29C51 chips on a single card. This interface provides an exchange of primary voice signal, secondary-channel data, feature-control information, and signaling status between each line circuit and the network controller. The exchange occurs every PCM frame simultaneously for all subscribers.

The chip's backplane interface connects the line card to the switching-system backplane. Two bidirectional PCM voice and data highways can be addressed, and these will operate at standard PCM rates with 24 to 64 time slots per direction for each 125-microsecond frame.

The 29C52 also has two signaling and control highways, with one channel active at any one time. Each signaling highway is configured with a PCM highway to form a line group. The signaling highways use a modified high-level data-link control protocol at the same speed as the PCM highways. All HDLC protocol control and response is carried out by the 29C52, including processing a variety of automatic responses regarding simultaneous reception, transmission errors, and address recognition.

The serial control structure in the HDLC protocol can



5. Microprocessor control flow. In smaller systems or where HDLC is not desired, a microprocessor can control the 29C52 through a direct-memory–address port. The associated routine follows a simple loop between the system backplane and the chip's control registers.

provide for fewer interconnections and has fewer signals to drive around the system than would a parallel-bus configuration. Moreover, a serial structure will cost less and present fewer noise problems.

Some of the penalties involved in this approach have been lessened with the 29C52 because the 4-MHz data rate helps to alleviate the bandwidth constraint inherent in serial channels. Also, the potential for errors in the serial structure is lessened with the HDLC protocol, which is compiled and interpreted by the 29C52. Acknowledgment requirements, error checking, and contention resolution between the two channels are HDLC features that improve data reliability.

The 29C52 accepts incoming HDLC-formatted commands for setting up voice calls. The opening and closing flag are standard formats. The address includes a 7-bit 29C52 identifier and a single control bit. The standard HDLC control byte is utilized only for bit 7, the poll-final response bit. The auxiliary control byte indicates the type of message in the information bytes and includes a reserved field to indicate the subscriber unit number. The feature-control commands follow and include receive and transmit highway and time-slot assignments. The cyclic redundancy error-checking code follows.

Each byte of information (FC_1 to FC_6, including the time-slot–assignment bytes) would be placed in a message first-in, first-out memory on the 29C52. As each frame passes, a feature-control command byte is sent out to the 29C51 of the appropriate subscriber line, and its time-slot data is sent to the correct location in the on-chip content-addressable memory.

The importance of reliability in system control links cannot be underestimated. The use of the HDLC protocol is a good start toward this goal since it can provide a response acknowledgment, as well as its own internal CRC code for error checking. In the event that one of the 29C52's line groups is disrupted, an external controller or line-card logic can switch all traffic to the functioning group, thereby identifying the problem channel.

Switching between the HDLC links has other important consequences for reliability. Duplicate and redundant modes can be used separately or together to provide single or double redundancy in control communications. When these modes are combined with the testing capability of the 29C51, automatic diagnostic testing and self-maintenance can become very comprehensive.

The voice-call setup can also be completed from the microprocessor port by following a simple program flow (Fig. 5). The microprocessor backplane command register (MBC) contains a bit used as an indication that a valid address byte is about to be located in the address register. The feature-control byte is placed in the microprocessor input/output buffer (MIOB) and is transferred once each frame to the feature-control register for that subscriber. After the byte has been transferred, the MIOB ready bit appears in status register 1, indicating that the previous byte has been transferred. After all bytes have been transferred, the frame-synchronization bit in the MBC register is cleared, and the processor can proceed.

The asynchronous portion of the 29C52 links its interface sections and provides the interface with a PBX microprocessor. The linking with synchronous circuitry occurs through the registers supporting receive and transmit information for the subscriber-line circuits.

Handling control data

Also, the IC has an instruction decoder for control information, which requires transmission to the subscriber circuits. This information includes both feature-control information and receive and transmit time-slot assignment for all channels. The instruction decoder also communicates the signaling command or status between the line circuits and the group controller at the other end of the signaling and control highways.

The microprocessor interface is designed with a full-feature multiplexed-bus interface, interrupt capability, and direct-memory–access request and acknowledge signals. With added circuitry controlling tone-key dialing to the line card, a 29C52 combined with an 8051 microprocessor could provide a complete switching function. In such an application, the system designer can determine the line features managed by the line-card processor because all status reports and control functions can also be supplied by a network processor on the serial HDLC control highways.

The 29C52 is addressed through a 7-bit location, which either can be set on its pins if no local processor is used or can be stored in an identification register on chip. The controller will then respond to that identification within the HDLC destination address. Driven by control software from either a remote group controller or a local processor, the chip is totally flexible concerning calling features, intercom capability, line lock-out, and system test and maintenance features. □

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Signal Processors

4

4 Signal Processors

PRELIMINARY

2920/2921
SIGNAL PROCESSOR

- 2920—User-Programmable/Erasable EPROM Program Memory (T_{CYC} = 600 ns)
- 2921—Mask-Programmable ROM Program Memory (T_{CYC} = 400 ns)

- Real Time Digital Processing of Analog Signals
- Stability and Accuracy of Digital Processing
- Nominal Signal Bandwidths from D.C. to 10 KHz
- Multiple Analog Inputs and Outputs
- On Chip A/D and D/A
- On Chip Program Memory
- On Chip Scratch Pad Memory
- Analog and/or TTL Output Waveforms, User Selectable
- Intellec® Development System Support:
 - — Compiler
 - — Assembler
 - — Simulator

The Intel 2920 Signal Processor is a programmable, single chip analog and digital signal processor specifically designed to replace analog subsystems in real time processing applications. The 2921 is an improved performance mask programmable (ROM) version of the 2920 which is pin compatible with the 2920. Its instruction set plus the high precision (25 bits) digital arithmetic logic unit provides the capability to implement very complex subsystems. Typical functions performed by the 2920 include: Lowpass and Bandpass filters with up to 20 complex pole and/or zero pairs; Threshold Detectors; Limiters; Rectifiers; up to 25-bit multiplication and division; approximations to nonlinear functions such as square law and logarithm; logical operations; input and Output multiplexing of signals; logical outputs for decision-type processing; and analog outputs for multifrequency oscillators, waveform generators, etc. In addition, several 2920's may be cascaded for very complex processing applications with no loss in throughput rate.

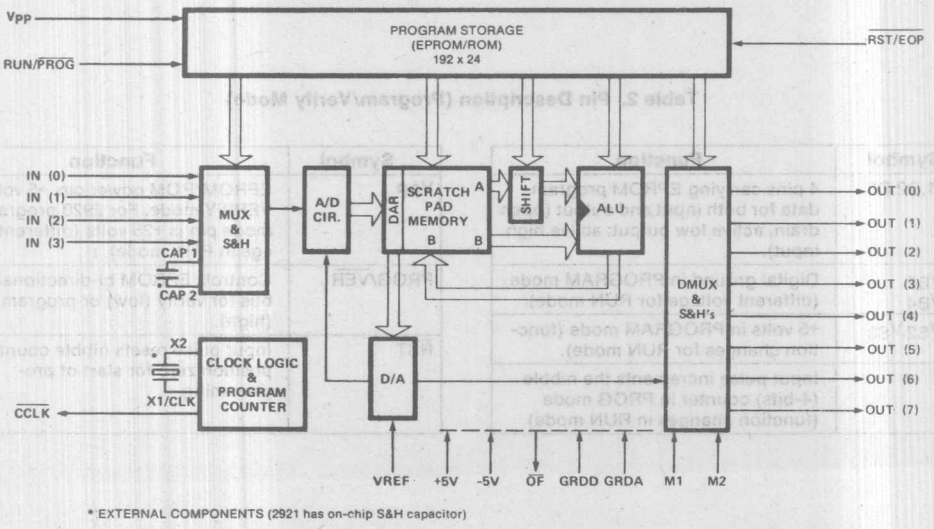


Figure 1. Functional Block Diagram (Run Mode)

Table 1. Pin Description (Run Mode)

Symbol	Function
OUT	Analog Output (0-7)
GRDA	Analog Ground
CAP_1 & CAP_2	External capacitor connections for the input signal sample and hold circuit. Not required for 2921.
VREF	Reference Voltage
IN	Analog Input (0-3)
V_{BB}	Most negative power pin set at -5 volts during run mode (different voltage in program mode).
X_2/CLK	Clock input when using external clock signals; oscillator input for external crystal when using internal clock.
X1	Oscillator input for external crystal when using internal clock.
GRDD	Digital ground.
V_{CC}	5 volts in run mode.
$\overline{CCLK}$	Internal fetch cycle clock output. The falling edge designates the START of a new PROM fetch cycle. $\overline{CCLK}$ is 1/16 of X_2/CLK rate.
RUN/$\overline{PROG}$	Mode control tied to GRDD in run mode.
$\overline{RST}$/$\overline{EOP}$	Reset Input and/or end of program output
$\overline{OF}$	Indicates an overflow in the current ALU operation (open drain, active low).
VPP	Programming Power (0 volts for run mode)
M1, M2	Output mode control (See Table 8)

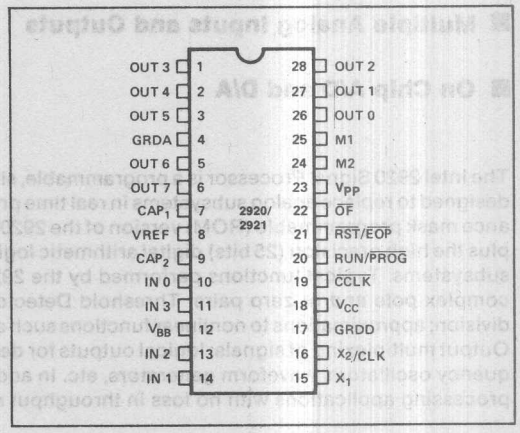


Figure 2. Run Mode Pin Configuration

Table 2. Pin Description (Program/Verify Mode)

Symbol	Function
D0,D1,D2,D3	4 pins carrying EPROM program data for both input and output (open drain, active low output; active high input).
V_{B1},V_{B2}, V_{B3},V_{B4}	Digital ground in PROGRAM mode (different voltage for RUN mode).
V_{S1},V_{S2},V_{S3}	+5 volts in PROGRAM mode (function changes for RUN mode).
$\overline{INCR}$	Input pulse increments the nibble (4-bits) counter in PROG mode (function changes in RUN mode).
VPP	EPROM/ROM power pin, +5 volts for VERIFY mode. For 2920 program mode pin is +25 volts (different voltage in RUN mode).
PROG/$\overline{VER}$	Controls EPROM bi-directional data bus for verify (low) or program (high).
$\overline{RST}$	Input pulse resets nibble counter to position zero for start of programming.

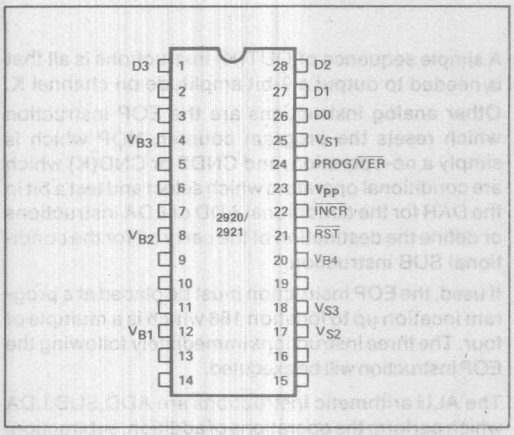


Figure 3. Program Mode Pin Configuration

FUNCTIONAL DESCRIPTION

The Intel 2920 is a programmable, single chip analog and digital signal processor which has been designed specifically to replace analog systems in real-time processing applications. The 2920 operates its analog circuitry simultaneously with the digital circuitry thereby achieving the efficiency and speed needed for real-time operation. Digital Circuitry includes: EPROM/ROM program storage, RAM scratch pad memory, clock and timing circuitry, binary scaler, and the arithmetic logic unit (ALU). The analog circuitry is composed of 4 analog inputs, an input multiplexer, an input sample and hold (S&H), A/D and D/A converters, an output multiplexer, 8 analog outputs, and buffered output S&H's.

Once the EPROM/ROM is programmed, the 2920 is ready for operation as an analog subsystem. The following signal flow and operations can be described with reference to the functional block diagram shown in Figure 1.

Clock and Timing Logic

The 2920/2921 can use an external clock or can generate its own clock with an external crystal placed across Pins 15 and 16. The program counter is incremented one instruction count for every 4 master clock cycles and continues to increment until it reaches a count of 191 or an EOP instruction is executed. Instructions are executed sequentially and no program jumps are provided. The sample rate is determined by the number of instructions in the program and the instruction cycle time. A 6.67MHz clock (600 nsec instruction cycle time) and a full 192 instructions will result in a sample rate of 8680Hz [clock rate (MHz) ÷ (4 x # of instructions)].

Program Storage and Control

The EPROM/ROM is made up of 192 words with 24-bits per word. Each 24-bit word contains 6 infields (see Table 3) which control the individual subsystems in the 2920.

RAM

The memory consists of a random-access read/write array organized as 40 words of 25-bits each. The address space is extended to provide constants and access to a register (DAR) for interfacing the memory-ALU with the analog conversion section. The RAM is a two port memory where the "A" location is Read Only and passes via a scaler to the ALU as one operand. The "B" location data passes to the ALU input as its second operand and the ALU result is written back to it. Both the RAM and the ALU represent data in two's complement format. All operations are performed in two's complement arithmetic. Program operations are simplified by assuming the binary point to the right of the sign bit.

An extended address space is used to generate constants within the program. It is accessed through the "A" port only and may be addressed using the last 16 locations of the "A" address field (i.e., "A" address 11XXXX). The constant is determined by the 4 least significant "A" address bits.

These 4 bits are treated as the 4 most significant bits at the input to the binary shifter. A sequence of extended addresses with shift operations can generate any constant up to 25 bits long.

The DAR is 9 bits wide and can be accessed in several ways. As a memory location, the DAR occupies the 9 most significant bit positions of the 25-bit word and can be accessed as "A" and/or "B" port. The DAR output is also tied directly to the D/A converter inputs and is used as a successive approximation register for A/D conversion under control of the analog function instruction fields. Each bit position of the DAR can also be selected and tested for conditional arithmetic operations.

Binary Shifter

The 2920 has a binary shifter between the memory port output and the ALU "A" operand input. This feature allows the "A" operand to be scaled by any magnitude between 2^{2} and 2^{-13} (left shift 2 to right shift 13). When a number is shifted right vacated bit positions are filled with the sign bit. (2's complement arithmetic shift). Shift op codes are shown in Table 4.

ALU

The Arithmetic-Logic Unit calculates a 25-bit result based on an operation performed on the scaled "A" and the "B" operands delivered from memory. The 25-bit result is written back into the "B" memory location near the end of the instruction cycle. The ALU has logic to accommodate the left shift scaling. For arithmetic operations, this logic is used to calculate a 25-bit result for normal operations and to maintain the sign bit when an overflow occurs. An overflow occurs only when the magnitude of the result is larger than the

largest number that can be stored in memory (25 bits). In that event, the result is set to the largest magnitude value with the correct sign. This overflow algorithm protects the continuity of the digitized analog signals and helps maintain the stability of the signal processing functions implemented. It is analogous to an overdriven amplifier going into saturation.

Instruction Set

The 2920 assembler uses the following program format to specify the 24-bit instruction word stored in the EPROM:



All processing subsystems are implemented using a combination of analog and digital instructions to input and output signals and/or data, and to realize the processing functions, respectively.

The analog input and output instructions are IN(K) and OUT(K), respectively. A sequence of IN(K) instructions followed by the sign conversion and amplitude conversion instructions CVTS and CVT(K) respectively are used to perform the input A/D conversion.

A simple sequence of OUT(K) instructions is all that is needed to output a 9-bit amplitude on channel K.

Other analog instructions are the EOP instruction which resets the program counter, NOP which is simply a no-operation, and CNDS or CND(K) which are conditional operators which select and test a bit in the DAR for the conditional ADD or LDA instructions or define the destination of the carry bit for the conditional SUB instruction.

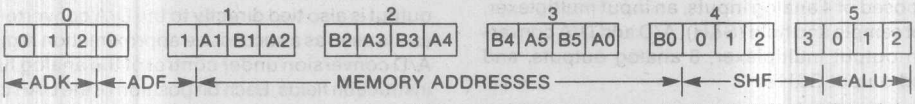
If used, the EOP instruction must be placed at a program location up to location 188 which is a multiple of four. The three instructions immediately following the EOP instruction will be executed.

The ALU arithmetic instructions are ADD,SUB,LDA which perform the operations of addition, subtraction, and data transfer respectively. When these instructions are conditioned, they may be used to perform multiplication or division by a variable or data dependent switching.

Other digital instructions include the absolute value ABS, the absolute value and add ABA, and the ideal limit instruction LIM.

These instructions and their corresponding op codes are detailed in Table 5.

Table 3. Nibble Organization for Loading Program



Note: The input pins for each nibble bit from left to right are D0, D1, D2, D3.

Table 4. Shift OP Codes

Operation	Mnemonic	Op Code				Scale Factor
		3	2	1	0	
Shift Right 13 Bits	R13	1	1	0	0	2^{-13}
Shift Right 12 Bits	R12	1	0	1	1	2^{-12}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
Shift Right 1 Bit	R01	0	0	0	0	2^{-1}
No Shift	R00	1	1	1	1	1
Shift Left 1 Bit	L01	1	1	1	0	2
Shift Left 2 Bits	L02	1	1	0	1	4

Table 5. Instruction Set and OP Codes

Mnemonics		Op-Codes[1]			Operations			Notes
Code	Condition	ALU	ADF	ADK				
Digital Instructions		0,1,2	0,1	2,1,0				
ADD		011	↑	↑	$(Ax2^N) + B \rightarrow B$			
SUB		101			$B - (Ax2^N) \rightarrow B$			
LDA		111			$(Ax2^N) + 0 \rightarrow B$			
XOR		000			$(Ax2^N) \oplus B \rightarrow B$			
AND		100			$(Ax2^N) \bullet B \rightarrow B$			
ABS		110			$\lvert(Ax2^N)\rvert \rightarrow B$			
ABA[11]		001	[3]	[3]	$\lvert(Ax2^N)\rvert + B \rightarrow B$			
LIM		010			$Sign(A) \rightarrow \pm F.S. \rightarrow B$[4]			
ADD	CND()[2]	011			$(Ax2^N) + B \rightarrow B$	IFF DAR(K) = 1		
					$B \rightarrow B$	IFF DAR(K) = 0		
SUB	CND()[2][8]	101			$B - (Ax2^N) \rightarrow B$ & $CY \rightarrow DAR(K)$	IFF $CY_P = 1$		[5]
					$B + (Ax2^N) \rightarrow B$ & $CY \rightarrow DAR(K)$	IFF $CY_P = 0$		
LDA	CND()[2]	111			$(Ax2^N) \rightarrow B$	IFF DAR(K) = 1		
					$B \rightarrow B$	IFF DAR(K) = 0		
ABA[11]	CND()[9]	001			$(Ax2^N) + B \rightarrow B$			
XOR	CND()[9]	000			$(Ax2^N) \oplus B \rightarrow B$			
Analog Instructions								
IN(K)		↑	00	0-3	Signal Sample from Input Channel K			
OUT(K)			10	0-7	D/A to Output Channel K			
CVTS			00	6	Determine Sign Bit			
CVT(K)			01	0-7	Perform A/D on Bit K			
EOP		[7]	00	5	Program Counter to Zero			[6]
NOP			00	4	No Operation			
CND(K)			11	0-7	Select Bit K for Conditional Instructions			
CNDS		↓	00	7	Select Sign Bit for Conditional Instructions			

Notes:
1. Op codes ALU and ADF are in binary notation, ADK is in decimal notation and represents the value "K" when appropriate.
2. CND() can be either CND(K) or CNDS testing amplitude bits or the sign bit of the DAR respectively.
3. Determined by analog instructions below.
4. B is set to full scale (F.S.) amplitude with the same sign as the "A" port operand.
5. The previous carry bit (CY_P) is tested to determine the operation. The present carry bit (CY) is loaded into the Kth bit location of the DAR. "Present carry (CY) is generated independent of overflow. It will represent the carry (CY) of a calculated 28-bit result."
6. EOP will also enable overflow detection if it was disabled during a program pass.
7. Determined by digital instructions above.
8. For SUB CNDS operation $\overline{CY} \rightarrow DAR(S)$.
9. Does not affect DAR. In this case, CND is used with XOR/ABA to enable/disable the ALU overflow saturation algorithm. An EOP instruction will also enable the ALU overflow saturation algorithm.
10. Clarification of CY_{OUT} sense for certain operations. For LDA, XOR, AND, ABS; $CY_{OUT} = 0$.
11. Recommend that the ABS & ADD instructions be used in place of ABA. The ABA instruction typically runs 2 MHz slower. The saturation logic, however can be set and reset at full speed.

ANALOG INPUTS

An analog input is digitized using a successive approximate technique. The successive approximations are software controlled. This allows the flexibility to convert a given input to the desired resolution. For example, an analog input can be converted with 9 bit resolution, but a TTL input needs only a 1 bit conversion to resolve a high or low digital level.

The input channels consist of four analog sampling switches which use a common sampling capacitor (external capacitor for the 2920, internal capacitor for the 2921). The external capacitor should be 500 pF to yield an offset of less than $-\frac{1}{2}$ LSB. The acquisition time should be approximately six times the RC time constant of the sample and hold circuitry (i.e., 500 pF x 1.5 kΩ = 750 nsecs).

The DAR is used as the successive approximation register, and as such should be cleared at the start of an analog input sequence. An input is selected and sampled using the IN(k) instruction, where k is the selected input (0 to 3). A series of consecutive IN's may be required to charge the sample capacitor to sufficient accuracy. For full 9 bit resolution the acquisition time (TIA) shown in the specifications table should be met. So, the number of consecutive IN's required is a function of the instruction cycle time and therefore a function of the chosen crystal or clock frequency. To calculate the number of IN(k) instructions needed to achieve less than -54 dB of input crosstalk, the following formula can be used:

$$\#\ IN's = (TIA_{max} \times f_{osc})/4$$

where TIA is the input acquisition time and f_{osc} is the crystal or clock frequency.

Once the input has been acquired (sampled and held), the successive approximation conversion sequence can begin. Normally the sign bit is converted first, and then each succeeding bit in order until the 9th bit (LSB) is converted. The digital word in the DAR (cleared at the start of the sequence) is converted by the DAC to a voltage which is one of the comparator inputs. The comparator compares the DAC voltage to the sampled and hold analog level. The comparator's output is routed via the DAR multiplexer to the appropriate bit position of the DAR. This new DAR value will propagate through the DAC to establish the new level to be compared for the bit conversion in the sequence. In between each successive bit conversion a 1.1 μ-sec (2920) or 800 nsec (2921) delay is required to allow the DAC time to settle. This delay is implemented in software by putting no operation (NOP) codes between conversions. Table 6A and B present analog I/O instruction requirements for the 2920 and 2921, respectively. An example input analog instruction conversion sequence, for the 2920, is presented in Table 7.

ANALOG OUTPUTS

An analog output is generated by converting the contents of the DAR into a voltage level using the DAC. The DAC output voltage is routed by the output multiplexer to one of eight internal sample and hold capacitors associated with the eight output buffers. This conversion and outputting is accomplished by a short sequence of instructions. First, the value to be output is moved to the DAR. Next, a short delay (a few NOP's) allows the DAC output voltage to settle. Then, the OUT(k) instruction selects the desired output (k = 0 through 7) and allows the output sample and hold to acquire the DAC output voltage. The sample and hold circuit has a required acquisition time (TOA) that is a function of voltage swing, which is met by a series of OUT (k) instructions. A rule that must be followed in outputting samples is that no outputting should be done while writing to the DAR. An example analog instruction conversion sequence for outputting (based on the analog output requirements presented in table 6-A) is presented in Table 8.

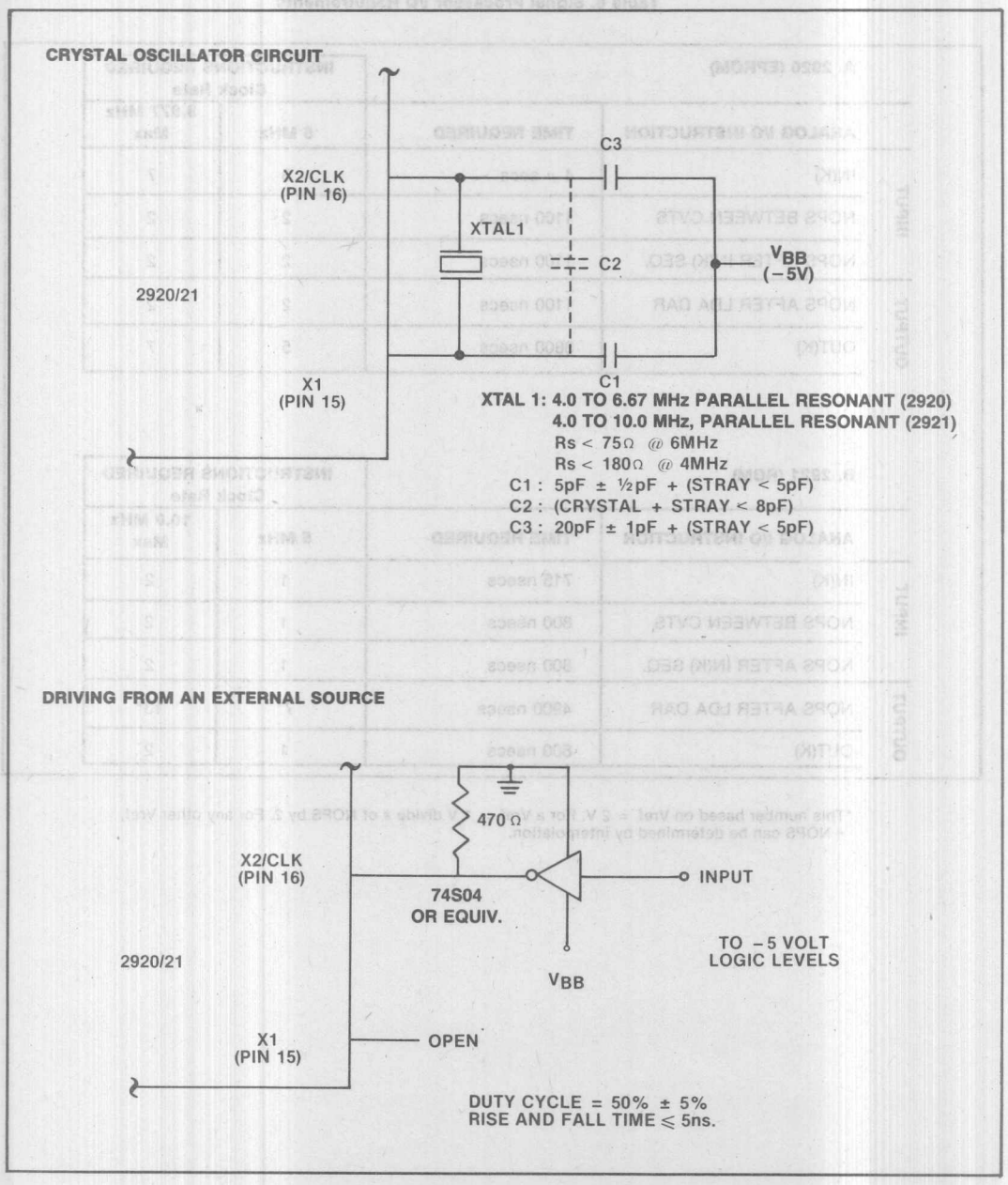


Figure 4. Clocking the 2920/21

Table 6. Signal Processor I/O Requirements

A. 2920 (EPROM)

	ANALOG I/O INSTRUCTION	TIME REQUIRED	INSTRUCTIONS REQUIRED Clock Rate 5 MHz	INSTRUCTIONS REQUIRED Clock Rate 6.677 MHz Max
INPUT	IN(K)	4 μ secs	5	7
	NOPS BETWEEN CVTS	1100 nsecs	2	2
	NOPS AFTER IN(K) SEQ.	1100 nsecs	2	2
OUTPUT	NOPS AFTER LDA DAR	1100 nsecs	2	2
	OUT(K)	3800 nsecs	5	7

B. 2921 (ROM)

	ANALOG I/O INSTRUCTION	TIME REQUIRED	INSTRUCTIONS REQUIRED Clock Rate 5 MHz	INSTRUCTIONS REQUIRED Clock Rate 10.0 MHz Max
INPUT	IN(K)	715 nsecs	1	2
	NOPS BETWEEN CVTS	800 nsecs	1	2
	NOPS AFTER IN(K) SEQ.	800 nsecs	1	2
OUTPUT	NOPS AFTER LDA DAR	4900 nsecs	7*	13*
	OUT(K)	800 nsecs	1	2

*This number based on Vref = 2 V. For a Vref = 1 V divide # of NOPS by 2. For any other Vref, # NOPS can be determined by interpolation.

Table 7. Example 2920 Input Sequence (6.67 MHz)

Digital	Analog	Digital	Analog
SUB DAR, DAR	IN(K)		CVT5
. . . .	IN(K)		NOP
. . . .	IN(K)		NOP
. . . .	IN(K)		CVT4
. . . .	IN(K)		NOP
. . . .	IN(K)		NOP
. . . .	IN(K)		CVT3
. . . .	NOP		NOP
. . . .	NOP		NOP
. . . .	CVTS		CVT2
. . . .	NOP		NOP
. . . .	NOP		NOP
. . . .	CVT7		CVT1
. . . .	NOP		NOP
. . . .	NOP		NOP
. . . .	CVT6		CVT0
. . . .	NOP		
. . . .	NOP		

Continue Next Column

where " " equals available digital instruction

Table 8. Example 2920 Output Sequence (6.67 MHz)

Digital	Analog
LDA,DAR,X,R0,	NOP
.	NOP
.	NOP
.	OUT(K)
.	OUT(K)
.	OUT(K)
.	OUT(K)
.	OUT(K)
.	OUT(K)
.	OUT(K)

where K = desired output, "." available digital instruction

Conditional operations should not immediately precede or follow an OUT instruction. Otherwise a CND(K) may affect the value of the Kth output.

TTL Output

The OUT(K) pins can be selected to be either analog out or TTL compatible as seen in Table 9. The analog mode allows the full 9-bit D/A output to be present. The LIM instruction can be used to yield a "0" or "1" decision for the TTL mode. This output can be presented to the OUT(K) pins and is compatible to a single TTL gate or equivalent. The internal threshold required is 1.5 volts for a high level output. An external pullup resistor to V_{CC} is also required.

Table 9. Output Mode for SIGOUT Pins as Function of M1 and M2

M1	M2	OUT Pins
5V	5V	0-7 Analog
5V	-5V	0-3 Analog, 4-7 TTL
-5V	5V	0-3 TTL, 4-7 Analog
-5V	-5V	0-7 TTL

Reference Voltage

The internal D/A converter requires a single positive reference voltage (VREF) to establish its voltage range. This user supplied reference can range from 1V to 2V. The resulting input and output signal voltage range is ±VREF. If the TTL output is required, VREF $\geq$1.5V is necessary. The minimum voltage step (LSB) of the D/A converter is $V_{REF}/256$ volts. Voltage variations on V_{REF} will appear as noise to the D/A converter. It is therefore necessary to provide a noise free voltage source for the reference. The input signal voltage range is (±VREF) -½ LSB.

EPROM PROGRAMMING

The 2920 EPROM in the programming mode is arranged as a 1152-by-4-bit memory. Each instruction (24 bits) is loaded as 6 nibbles (4 bits) as seen in Table 3. Figure 6 shows the timing relationships of the signals required to program and verify the EPROM contents. In the program mode all voltages are referenced to V_{BB} which is set to digital ground, thereby allowing TTL logic to be used for controlling the programming cycle. The D pins are bidirectional with the direction controlled by the PROG/VER pin. A high level at the PROG/VER pin switches to input mode, a low to output mode (see Figure 6). This feature allows the programmed data to be verified before going on to the next address.

The internal nibble counter is incremented during the falling edge of INCR. 1152 INCR transitions will complete the full program cycle. To initialize at address (nibble) 0, RST must be pulsed low, then INCR can be issued. From then on, programming is accomplished according to Figure 6.

The RUN/PROG pin must be tied to V_{BB} and VSP should be pulsed between +5V and $+25 \pm 1$V at 15mA maximum. The D pins have an open drain in the output direction.

2920 DEVELOPMENT SUPPORT TOOLS

Support tools for the 2920 are based on the Intellec® Microcomputer Development Systems. A 2920 Software Support Package (SPS-20) consisting of the Signal Processing Applications Software/Compiler (SPAS-20), the 2920 Software Simulator, and the 2920 Assembler is available to facilitate design and development efforts.

The 2920 Signal Processing Applications Software/Compiler is an interactive tool for designing software to be executed on the 2920 Signal Processor. The compiler accepts English-like statements from the user and generates 2920 assembly language code.

The assembler translates symbolic 2920 assembly language programs into the machine operation codes. The user can load the codes into the 2920 simulator or to the Universal EPROM Programmer for programming the 2920 itself.

The simulator, operating entirely in software, allows the user to test and debug 2920 programs. The user can specify input signals, simulate program execution, set up breakpoints, display input and output, display and alter the contents of the 2920 registers and memory locations, and graph the output waveforms.

The compiler, assembler and simulator enable the designer to develop and test an entire program without programming the device. The 2920 designer works at the Intellec® Microcomputer Development System rather than at a breadboard. The development system facilitates the designing and testing of 2920 applications.

The SDK-2920 contains all of the components required to assemble a complete single board microcomputer system for programming and evaluation of the 2920 Analog Signal Processor. The 8085/8041A microcomputer-based program development section allows you to immediately enter programs in 2920 assembly mnemonics, translate them to 2920 object code, and program the on-board 2920 EPROM. The kit supports basic filing options such as up/down loading to/from an Intellec, audio cassette, and line printer. The SDK-2920 also provides the user with a 2920 run mode section allowing real-time execution of a programmed 2920. This section comes complete with BNC connectors and Intel's 2912 PCM line filters required for one input and one output network. The kit supports optional input and output circuitry on the run mode section.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias −40°C to +85°C
Storage Temperature −65°C to +150°C
V_{CC} Supply with Respect to GRDD +5.5V
V_{BB} Supply with Respect to GRDD −5.5V
GRDA Supply with Respect to GNDD +/− 0.05V
Analog Inputs with Respect to GRDA −5.5V to +5.5V
Power Dissipation 2920 (at 0°C) 1W
2921 (at 0°C) 1.5W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (Run Mode) (T_A = 0°C to +70°C; V_{CC} = 5V ±5%; V_{BB} = −5V ±5%)

ANALOG (IN(K), OUT(K))

Symbol	Parameter	2920 Min	2920 Typ	2920 Max	2921 Min	2921 Typ	2921 Max	Units	Test Conditions
Z_I	Input Impedance	100			200			MΩ	Unsampled input
Z_{SH}	S&H Impedance	0.7	1.2	2.0	5	10	20	MΩ	Series resistance with S&H
	A/D Resolution			9			9	bits	
	Input Differential Linearity		±.75	±2.0		±.5		LSB	2V Vref
	Input Integral Linearity		±.75	±2.0		±1.0	±2.5	LSB	2V Vref
T_A	Aperature		±7.5			±7.5		nsec	
X_I	Input Crosstalk			−54		−60		dB	Input to input
V_{ID}	Input Droop Rate			50			50	μV/μs	500 pF cap.
V_{IR}	Input Voltage Range			±VREF			±VREF	V	Note 1
V_{IOS}	Input Zero Offset	.1				±10		mV	
I_{IZC}	Input Zero Crossing Error		.5	2		0		LSB	2V Vref
G_I	Input Gain	.95	1	1.05	.95	1.0	1.05	V/V	
	Input Gain Error		2			0		%	Ratio of neg. & pos. gains
T_{IA}	Input Acquisition Time[2]	3.6			.7			μs	9 bit resolution
Z_O	Output Impedance		800			800		Ω	During output
I_O	Output Drive Current		350			350		μA	
	D/A Resolution			9			9	bits	
	Output Differential Linearity		±.2	±1		±.5		LSB	2V Vref
	Output Integral Linearity		±.5	±2		±1		LSB	2V Vref
X_O	Output Crosstalk		−59	−45		−59	−45	dB	Output to output
V_{OD}	Output Droop Rate			7			7	$\frac{\mu V}{\mu sec}$	
V_{OR}	Output Voltage Range	−2		+2	−2		+2	V	
V_{OOS}	Output Zero Offset	0	−16	−70		±10	±40	mV	
V_{OZC}	Output Zero Crossing Error			±1			±1	LSB	2V Vref
G_O	Output Gain	.8	.885	1.0	.95	1.0	1.05	V/V	
	Output Gain Error		.55	1.0		—		%	Ratio of neg. & pos. gains
T_{OA}	Output Acquisition Time[3]	4.2			.375		.75	μs	9-bit resolution
G_T	Throughput Gain		.885			1.0		V/V	A/D to D/A
VREF	Voltage Reference Level			2.0			2.0	V	
I_{VR}	Voltage Reference Current		150	220		400		μA	2V Vref
C_L	Max. Capacitance Load			50			50	pF	

Notes: 1. V_{IR} = ± Vref for accurate conversion. Input levels outside of ±Vref will be converted as ± full scale.
2. For 500 pF capacitor (2920 only)
3. Minimum corresponds to 1V Vref, maximum to 2V Vref.

DIGITAL ($\overline{OF}$,$\overline{CCLK}$,$\overline{RST}$/$\overline{EOP}$,X2/CLK, OUT(K) in TTL Mode)

Symbol	Parameter	2920 Min	2920 Typ	2920 Max	2921 Min	2921 Typ	2921 Max	Units	Test Conditions
I_{IL}	Low Level Input Current			10			10	μA	VIN < VIL Driving $\overline{RST}$
I_{IH}	High Level Input Current			10			10	μA	VIN < VIH Driving $\overline{RST}$
V_{IL}	Input Low Voltage			0.8			0.8	V	DC trigger level
V_{IH}	Input High Voltage	2.0			2.0			V	DC trigger level
V_{IXL}	Input Low Voltage, X2/CLK	−5.0		−4.5	−5.4	−5	−4.6	V	
V_{IXH}	Input High Voltage, X2/CLK	−.3		0	−2.0	0	0	V	
I_{OL}	Output High Current	1.7	2		1.7			mA	V_{OL} = .4V
I_{OH}	Output Low Current			10			10	μA	

POWER DISSIPATION

I_{CC}	Operating Current		30	50		50	80	mA	V_{CC} = 5.25V
I_{BB}	Operating Current		110	150		150	200	mA	V_{BB} = −5.25V

A.C. CHARACTERISTICS (Run Mode)

F_{OSC}		4.0		6.67	1		10	MHz	Oscillator frequency
T_{CYC}	Instruction Cycle Period	600		1000	400		4000	ns	4 clock cycles
T_{CE}	Cycle Start to EOP Valid			255	100	200	240	ns	
T_{EW}	EOP Pulse Width	TCYC -150			360		450	ns	
T_{OW}	OF Pulse Width	TCYC -100			360		450	ns	
T_{CW}	CCLK Pulse Width	TCYC -65			360		450	ns	
T_{CO}	Cycle Start to OF Valid			TCYC +95	360		450	ns	

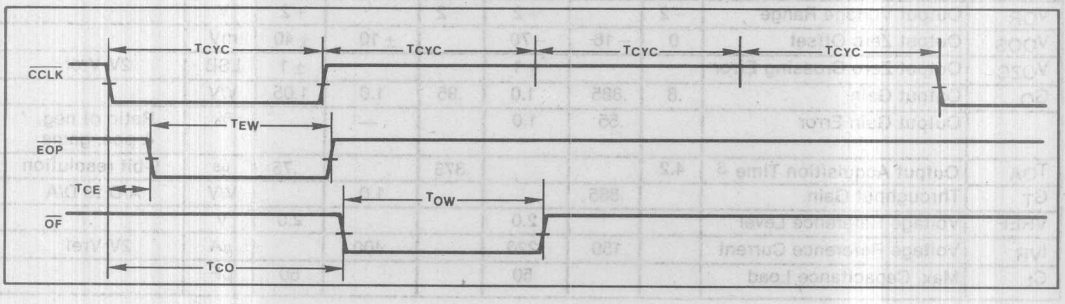


Figure 5. Run Mode Timing

D.C. CHARACTERISTICS (Program/Verify Mode) (T_A = 0°C to +70°C; V_{SS} =5V; V_{BB} = 0V)

Symbol	Parameter	2920 Min	2920 Typ	2920 Max	2921 Min	2921 Typ	2921 Max	Units	Test Conditions	
I_{TL}	Low Level Input Current			10			10	μA	$V_{IN} < V_{IL}$	
I_{IH}	High Level Input Current			10			10	μA	$V_{IN} < V_{IH}$	
V_{IL}	Input Low Voltage			0.8			0.8	V		
V_{IH}	Input High Voltage	2.0			2.0			V		
V_{OL}	Output Low Voltage			0.8			0.8	V	I_{OL} = 2.5mA	
I_{SP}	Program Pulse Current			16	—	—	—	mA	Data Input=0000	
V_{P1}	Program Pulse ON Voltage	24	25	26	—	—	—	V		2920
V_{P2}	Program Pulse OFF Voltage		5		—	—	—	V		Only
POWER DISSIPATION (Program/Verify Mode)										
I_{SS}	Operating Current		100			—		mA	V_{SS} = 5V+10%	

A.C. CHARACTERISTICS (Program/Verify Mode) (T_A = 0°C to +70°C; V_{SS} =5V; V_{BB} = 0V)

		2920			2921				
T_{RW}	Reset Pulse Width	1000			1000			ns	
T_{RS}	Reset to Increment Set-up	200			200			ns	
T_{RH}	Reset Hold	300			300			ns	
T_{IW}	Increment Pulse Width	1			1			μs	
T_{VP}	Data in Set-Up to Prog. Pulse	2			2			μs	
T_{PW}	Program Pulse Width (2920)	50		55	—	—	—	ms	
	Verify Hold Time (2921)	—	—	—	50		55	ms	
T_{PV}[1]	Program to Verify Settling	1			1			μs	
T_{ACC}	Verify Access Time	20			20			μs	
T_{VI}	End of Verify to Increment	100			100			ns	

Note: 1. Vpp must not undershoot 5V by more than 0.5V. Add undershoot settling time to T_{PV}.
***25V program pulse must NOT be applied to 2921.**

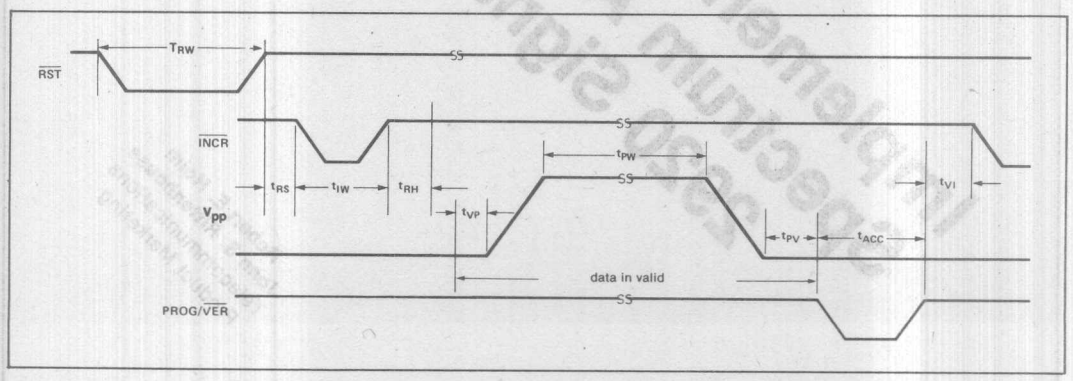
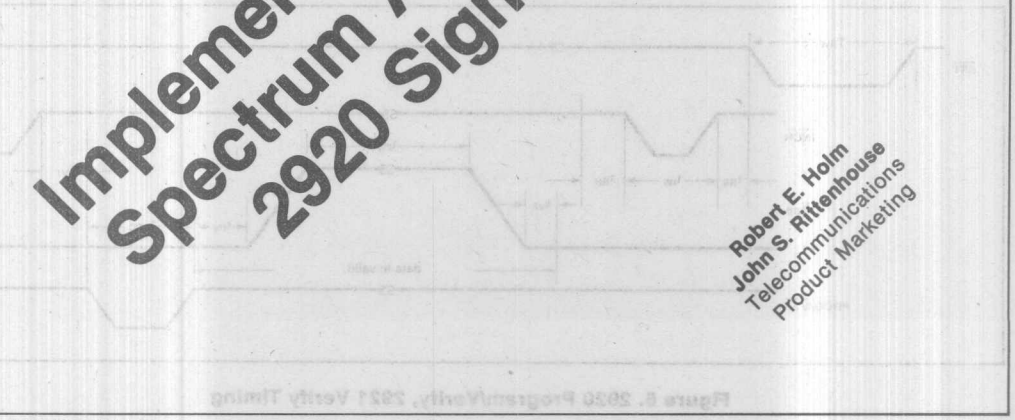


Figure 6. 2920 Program/Verify, 2921 Verify Timing

February 1980

Implementation of a Scanning Spectrum Analyzer Using the 2920 Signal Processor

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Telecommunications
Product Marketing



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1.0 INTRODUCTION

The purpose of a scanning spectrum analyzer is to determine the long term spectral characteristics of an analog signal. This is done by sweeping the input signal through a bandpass filter and displaying the filter output as a function of time. This application note describes the implementation of a sampled data scanning spectrum analyzer using the 2920 Signal Processor.

A scanning spectrum analyzer embodies many of the functions which can be found in a broad class of analog applications. These functions include: lowpass and bandpass filters, multipliers (mixers), detectors, and oscillators. The spectrum analyzer is a useful circuit which lends itself to applications such as speech processing, industrial control, medical electronics, signal detection, and signal processing.

The implementation of a spectrum analyzer using a sampled data system requires an understanding of sampling theory and digital signal processing as well as the ability to specify the system in analog terms. A basic review of sampling theory is provided in Section 2. Section 3 describes the 2920 Signal Processor. Section 4 describes the block diagram of the spectrum analyzer and discusses the design considerations. Once the block diagram of the application is complete, it is relatively straightforward to implement each subsystem as a block of code in the 2920 Signal Processor. Section 5 describes the implementation of the spectrum analyzer then gives a more detailed look at the actual design process using the signal processor resulting in the final 2920 assembly language program. A complete listing of the spectrum analyzer program is given in Appendix A.

2.0 SAMPLED DATA SYSTEM

Sampled data systems can be implemented using either analog or digital processing techniques or both. Examples of analog processing include transversal filters using CCD or bucket brigade shift registers and analog tap weights to implement transfer characteristics. The identical characteristics can also be implemented using digital processing. Since the use of digital processors are of interest here, it is useful to investigate the elements of a general purpose signal processor using a digital implementation.

2.1 Block Diagram Description

The block diagram shown in Figure 2.1 illustrates the basic blocks of a general purpose sampled data system using a digital signal processor. In this configuration it is assumed that both the input and output signals will be analog. (This is not a necessary condition since digital signals can be considered a special type of analog signal and processed accordingly.) The following paragraphs describe the function of each block in Figure 2.1.

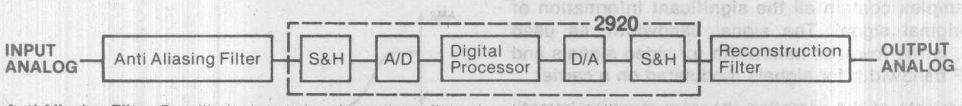
Anti-Aliasing Filter — This filter is used to bandlimit the incoming analog signal prior to sampling (thus a continuous analog filter is used) so that distortion terms (aliasing noise) due to the sampling process are minimized.

Input Sample and Hold (S&H) — The filtered input signal is sampled at an instant in time and the resulting sampled amplitude is held long enough for subsequent processing such as analog/digital conversion (Hold time ⩽ the sample period).

Input Analog to Digital Converter (ADC) — The held analog voltage is converted to a digital word by comparing the voltage to discrete thresholds representing the digital words.

Digital Processor — This can be a general purpose processor or one specifically built to perform a predetermined algorithm. Typically, a general purpose microprocessor can be programmed to perform any function but the resulting execution time is too limiting for most real-time applications. A programmable digital signal processor such as the 2920 eliminates this problem because it is designed specifically for high speed signal processing while at the same time preserving its general purpose nature.

Digital to Analog Converter (DAC) — The processed digital words are converted back to analog using the DAC. Again, the analog signal is approximated by



Anti Aliasing Filter: Bandlimits input signal to reduce distortion due to sampling

S & H: Sample and hold performs sampling process and holds data sufficiently long for processing

A/D: Analog to digital conversion, generates a digital word to represent held analog voltage

Digital Processor: Implement transfer function using digital processing (under software control)

D/A: Converts digital words to analog voltages

Reconstruction Filter: Smooths D/A or S & H waveforms to recover continuous analog output signal

Figure 2.1. Elements of a Sampled Data System Using Digital Processing

discrete amplitude levels (as in the ADC). In addition, the DAC output weights the signal output in the frequency domain thereby causing some signal distortion.

Output Sampler — One method of reducing the output frequency distortion is to resample the output signal using a very narrow sample width. The sampler takes the DAC held output and resamples it with narrow sample pulses.

Reconstruction Filter — Since the desired output signal is a continuous representation of the processed input signal, it is necessary to remove high frequency components resulting from the DAC or sampler outputs. This in effect smooths the analog output from sample to sample. A lowpass filter is used to perform the signal "reconstruction."

The process of sampling a signal introduces certain amounts of distortion called aliasing noise. The conversion of the analog samples to digital words is done with an analog to digital converter (ADC). This circuit represents the analog signal with a digital word which corresponds to a discrete amplitude approximation to the signal. This process also introduces a distortion term called quantization noise. By properly designing the sampled data system, these distortion or "noise" terms can be made insignificantly small so that the sampled data system closely represents the analog equivalent system with all the advantages of digital processing.

2.2 Sampling Theory

A digital signal processor requires the conversion of the input analog signal to a digital signal. Inherent in this analog-to-digital conversion is the sampling of the continuous input signal. As would be expected, the method and rate of sampling of the input signal affect the information content of the sampled signal so that some degree of distortion is incurred when the input signal is analog reconstructed from the digital data samples.

A sampling theorem that relates the minimum required sampling frequency to the signal bandwidth can be stated as follows. If a signal f(t) (a real function of time) is sampled instantaneously at regular intervals and at a rate higher than twice the signal bandwidth that includes all the significant frequency components, then the samples contain all the significant information of the original signal. The signal bandwidth, as used above, is the lowpass bandwidth for video signals and the RF bandwidth for signals modulated on a carrier.

Two aspects of the sampling theorem must be investigated prior to the selection of a sampling frequency.

- What is the effect of finite-width samples (vs instantaneous samples) on the information content of the samples?
- How is it determined that the signal bandwidth contains all significant frequency components?

To digitize each sample, it is necessary that the sample pulse amplitude be constant during the sample to allow a digital word to be generated that represents the sampled analog value. This process is called "square-topped sampling" and can be realized using a sample-and-hold circuit. Because the 2920 works with digitized samples, the square-topped sampling is the process of interest here.

Assuming an input spectrum $F(j\omega)$, the output spectrum for square-topped sampling $F_{sT}(j\omega)$ is

$$F_{sT}(j\omega) = \left(\frac{\tau}{T}\right)\left(\frac{\sin(\omega\tau/2)}{\omega\tau/2}\right)\sum_{n=-\infty}^{\infty} F\,j(\omega - n\omega_s)$$

From this equation we note that the gain is a continuous function of frequency defined by

$$\left(\frac{\tau}{T}\right)\left(\frac{\sin(\omega\tau/2)}{\omega\tau/2}\right)$$

The time- and frequency-domain plots for the square-topped sampled signals are shown in Figure 2.2. It is clear in 2.2(d) that the sampling process acts as a lowpass filter with a sin x/x amplitude response. If this filter response is not constant across the signal bandwidth, some information content of the signal will be lost due to rolloff distortion.

The amount of spectral overlap seen between the lowpass spectrum and that centered about the sampling frequency is referred to as aliasing noise. The effect of sample rate on aliasing noise for a given input spectrum can be clearly seen in Figure 2.3. Note that the amount of overlap increases as the sampling frequency is

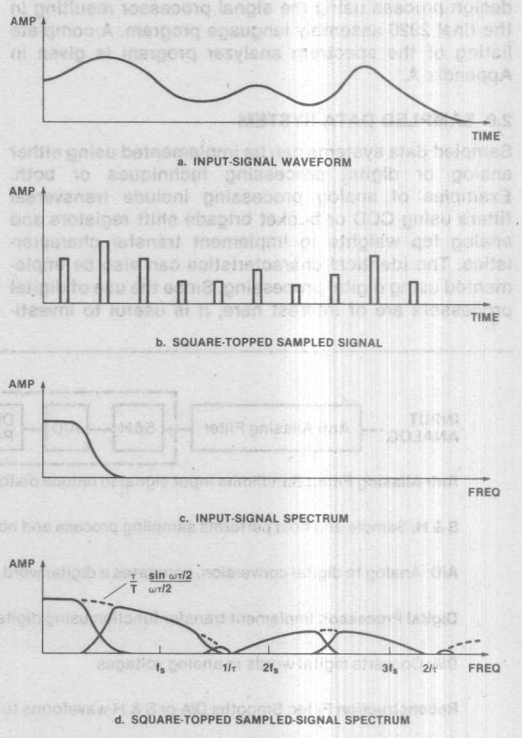


Figure 2.2. Analysis of a Sampled Signal

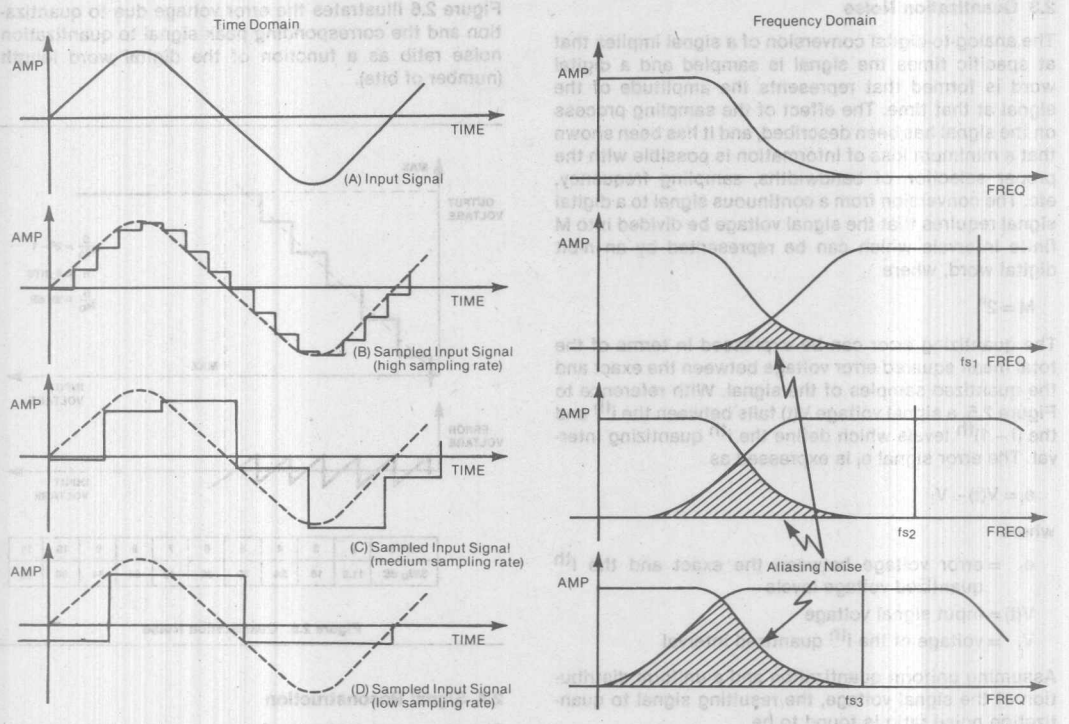


Figure 2.3. Effects of Sampling Rate on Aliasing Noise

decreased. In a similar manner, for a fixed sampling frequency, the overlap could be reduced by increasing the filter rolloff before sampling (anti-aliasing filter). Figure 2.4 illustrates the overlap for several popular filter types. These tradeoffs between filter selectivity and sampling frequency will be used in the spectrum analyzer design.

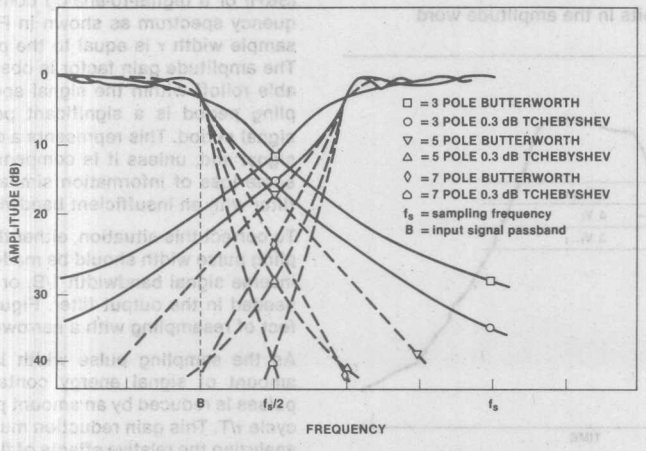


Figure 2.4. Effects of Filtering on Aliasing Noise

2.3 Quantization Noise

The analog-to-digital conversion of a signal implies that at specific times the signal is sampled and a digital word is formed that represents the amplitude of the signal at that time. The effect of the sampling process on the signal has been described, and it has been shown that a minimum loss of information is possible with the proper selection of bandwidths, sampling frequency, etc. The conversion from a continuous signal to a digital signal requires that the signal voltage be divided into M finite intervals which can be represented by an n-bit digital word, where

$$M = 2^n$$

The quantizing error can be expressed in terms of the total mean squared error voltage between the exact and the quantized samples of the signal. With reference to Figure 2.5, a signal voltage V(t) falls between the i^{th} and the $(i-1)^{th}$ levels which define the i^{th} quantizing interval. The error signal e_i is expressed as

$$e_i = V(t) - V_i$$

where

e_i = error voltage between the exact and the i^{th} quantized voltage levels

$V(t)$ = input signal voltage

V_i = voltage of the i^{th} quantized interval

Assuming uniform quantization and a uniform distribution of the signal voltage, the resulting signal to quantization noise ratio is found to be

$$S/N_Q = M^2 - 1$$

or represented as a logarithm

$$S/N_Q = (6)\,(n)\ dB$$

where

S is the peak signal power

N_Q is the mean quantization noise

M is the number of quantization levels $= 2^n$

n is the number of bits in the amplitude word

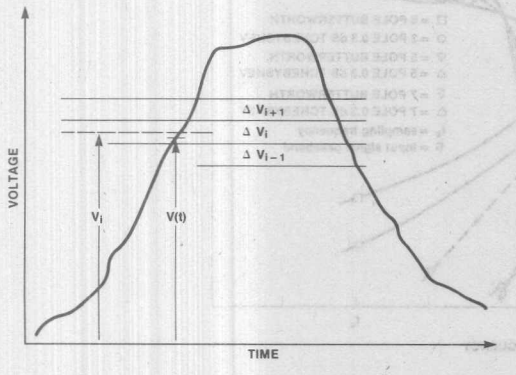
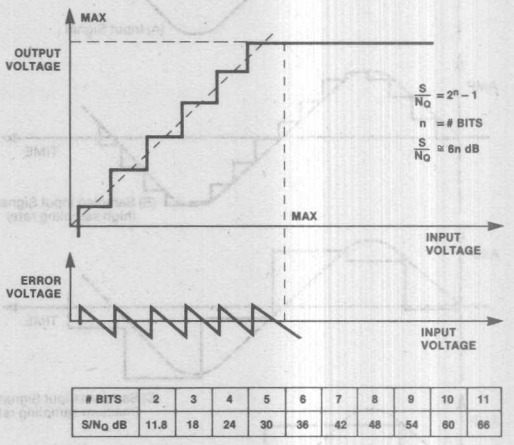


Figure 2.5. Quantization Step

Figure 2.6 illustrates the error voltage due to quantization and the corresponding peak signal to quantization noise ratio as a function of the digital word length (number of bits).



# BITS	2	3	4	5	6	7	8	9	10	11
S/N_Q dB	11.8	18	24	30	36	42	48	54	60	66

Figure 2.6. Quantization Noise

2.4 Signal Reconstruction

Signal reconstruction is the process that extracts the desired signal from the periodic samples at the output of the sampled data system. These samples may be the original samples at the output of the sample-and-hold or they may have been formed after linear or digital processing.

The basic assumption here is that a signal, which has been sampled and held for digital processing, is now to be converted back to analog form with minimum loss of information. The output of a sample-and-hold circuit (S&H) or a digital-to-analog converter (DAC) has a frequency spectrum as shown in Figure 2.7(a), where the sample width τ is equal to the period of the sample T. The amplitude gain factor is observed to have a noticeable rolloff within the signal spectrum when the sampling period is a significant portion of the shortest signal period. This represents a distortion of the output signal and, unless it is compensated for, it will cause some loss of information similar to that of a lowpass filter with an insufficient bandwidth.

To correct this situation, either the reconstruction sampling pulse width should be made narrow relative to the inverse signal bandwidth 1/B, or a sin x/x correction is needed in the output filter. Figure 2.7(b) shows the effect of resampling with a narrower pulse.

As the sampling pulse width is made narrower, the amount of signal energy contained in the sampling pulses is reduced by an amount proportional to the duty cycle τ/T. This gain reduction must be considered when analyzing the relative effects of fixed offsets, overshoot, ringing, and other spurious signals that degrade the desired signal.

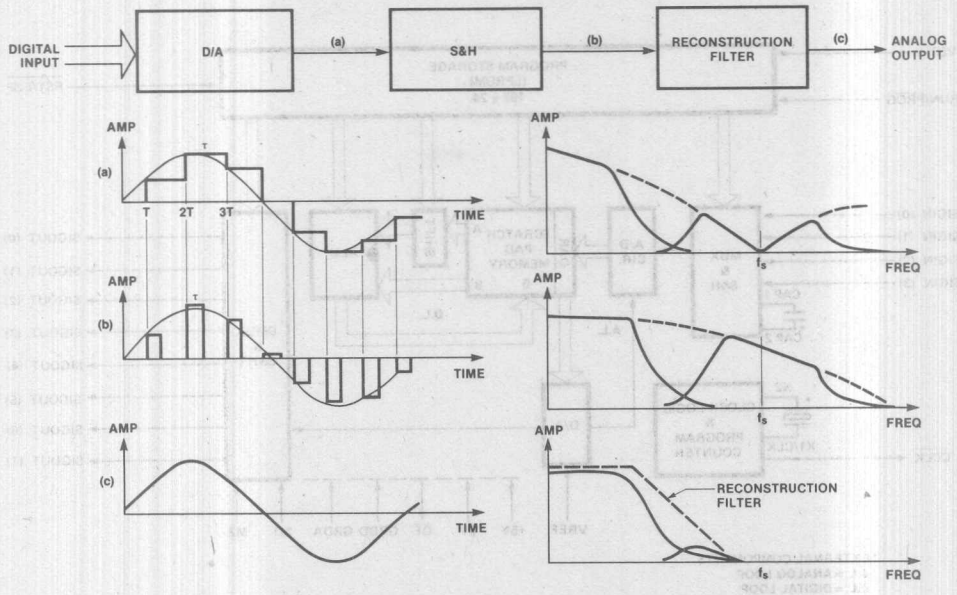


Figure 2.7. Analog Signal Reconstruction

When the data samples have been established, they are passed through a reconstruction lowpass filter that removes the high-frequency components of the sampled signal (Figure 2.7(c)). The purpose of the output lowpass filter is primarily to remove the high-frequency spectra caused by the output sampling. It can also be used to help shape the amplitude and phase response of the output network. The Intel 2912 PCM line filter can sometimes be used for both anti-aliasing and signal reconstruction filtering. The 2912 reconstruction filter also provides sin x/x correction.(1)

3.0 2920 SIGNAL PROCESSOR DESCRIPTION

The 2920 performs all the functions illustrated in Figure 2.1 beginning with the input S&H and ending with the output S&H. In addition, 4 input lines and 8 output lines are multiplexed to give the 2920 the capability of realizing several circuits, or one circuit with multiple inputs and outputs. A functional block diagram of the 2920 is shown in Figure 3.1.

The functions of the 2920 are controlled by the instructions stored in its 192-word EPROM. Each instruction is 24 bits long and is split into 5 fields, with each field controlling a subsystem of the 2920. In order to maintain a constant sample rate, the execution time for each instruction is identical and there is no conditional branching. The sample rate is determined by the program length and the instruction cycle time, which is four clock cycles or 400 ns at the maximum 10 MHz clock rate. A full 192 instruction program, running at 10 MHz, results in a 13 kHz sample rate. This allows for a signal bandwidth of approximately 4 kHz (maximum of 6.5 kHz with a rectangular filter). A shorter program will yield a higher sample rate.

3.1 Analog Operations

The 2920 input and output operations are under program control. To acquire an input signal, one of the 4 input lines is selected and the signal sampled and held. The resulting sample is then converted to digital form using a successive approximation A/D conversion. The result of the conversion can be up to 9 bits (a sign bit and 8 amplitude bits). However, since the A/D conversion is under program control, the conversion could consist of only a single bit which might be used to read a logical input for example.

The result of the A/D conversion is stored in the DAR. This register provides the interface between the analog and digital sections of the 2920. After the A/D conversion, the digital word in the DAR can be moved to a scratch pad RAM location for further processing. The DAR is also used for the output operation where the 9 most significant bits of the value to be output are loaded into the DAR. The DAR drives the D/A converter, which is connected via the output demultiplexer to one of the 8 output S&H circuits.

3.2 Digital Operations

The digital loop, shown in Figure 3.1, includes the 2 port, 40 word scratch pad RAM, a binary shifter, and the ALU. Two 25-bit words are fetched simultaneously from the 40 possible RAM locations. The data from the A port is

(1) R. E. Holm, "Data Conversion, Switching, and Transmission Using the Intel 2910A/2911A Codec and 2912 PCM Filter," Intel AP-64, p. 35.

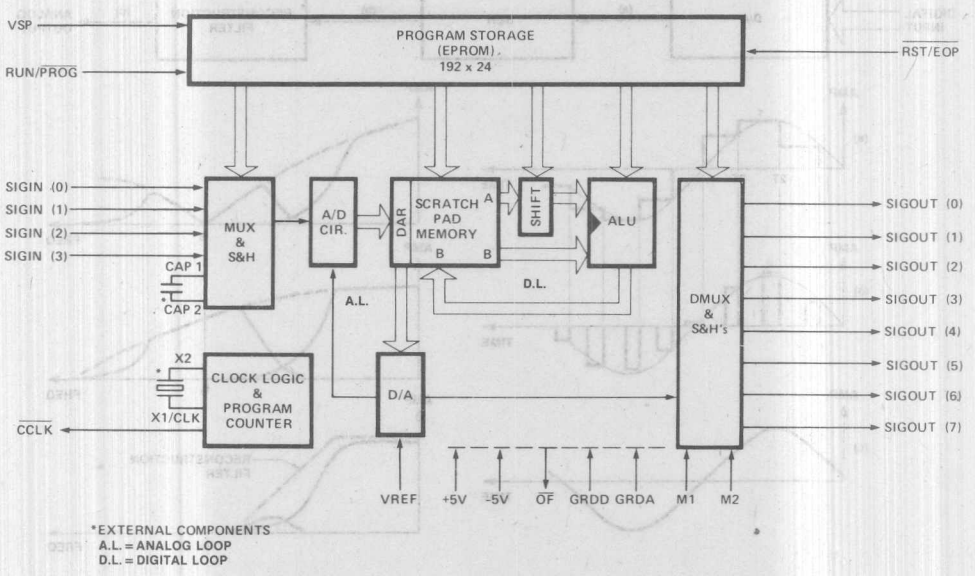


Figure 3.1. Functional Block Diagram (Run Mode)

passed through the binary shifter, which allows scaling from 2^2 (a 2-bit left shift) to 2^{-13} (a 13-bit right shift). The scaled A value and the unscaled B value are then passed on to the ALU. Sixteen internally available 4-bit constants are also accessible via the A port.

The ALU operates on the two values using the digital instructions specified by the program, and produces a 25-bit result. This result is then stored in the RAM location specified by the B address.

Digital and analog operations can execute simultaneously. For example, while doing a 9-bit A/D conversion, it is possible to implement a 5 pole lowpass filter with the digital section of the 2920. What gives the 2920 real-time processing capability is the ability to do the dual memory fetch, binary shift, ALU processing, and write back to memory as well as an analog operation in one instruction cycle (400 ns with a 10 MHz clock).

3.3 The 2920 Instruction Set

The following format is used by the 2920 assembler to specify the 24-bit instruction word stored in the EPROM:

ALU INSTRUCTION	B ADDRESS (DESTINATION)	A ADDRESS (SOURCE)	SHIFT CODE	ANALOG INSTRUCTION

Processing subsystems are implemented using a combination of analog and digital instructions.

The analog input and output instructions are IN(K) and OUT(K). To acquire a sample of the input signal, a sequence of IN(K) instructions is used. The A/D conversion is performed by the sign conversion and amplitude conversion instructions CVTS and CVT(K) respectively. A sequence of OUT(K) instructions will place a 9-bit amplitude on output channel K. Other analog instructions are the EOP instruction which resets the program counter to zero after the next three instructions are executed, NOP which is simply a no-operation, and CNDS or CND(K) which are conditional operators which test a bit of the DAR for the conditional ADD or LDA instruction, or define the destination of the carry bit for the conditional SUB instruction.

The arithmetic operations are ADD, SUB, and LDA which are addition, subtraction, and data transfer (load) respectively. These instructions may be modified with a conditional operator and used to perform multiplication or division by a variable or data dependent (conditional) switching. Other digital instructions are the absolute value ABS, the absolute value and add ABA, the ideal limit instruction LIM, and the logical instructions XOR and AND. Two special instructions, ABA CND() and XOR CND(), are used to disable and enable, respectively, the ALU overflow saturation algorithm. The instruction set is given in Table 3.1. The 2920 internal constants and scalar mnemonics are listed in Table 3.2 and Table 3.3 respectively.

TABLE 3.1. INSTRUCTION SET AND OPERATIONS

Mnemonics Code / Condition	Operations		
Digital Instructions			
ADD	$(A \times 2^N) + B \longrightarrow B$[1]		
SUB	$B - (A \times 2^N) \longrightarrow B$		
LDA[3]	$(A \times 2^N) + 0 \longrightarrow B$		
XOR[3]	$(A \times 2^N) \oplus B \longrightarrow B$		
AND	$(A \times 2^N) \cdot B \longrightarrow B$		
ABS[3]	$[(A \times 2^N)] \longrightarrow B$		
ABA	$[(A \times 2^N)] + B \longrightarrow B$		
LIM	$Sign(A) \rightarrow \pm$ F.S. $\rightarrow B$[4]		
ADD CND()[2]	$(A \times 2^N) + B \longrightarrow B$		IFF DAR(K) = 1
	$B \longrightarrow B$		IFF DAR(K) = 0
SUB CND()[2][7]	$B - (A \times 2^N) \longrightarrow B$	& CY → DAR(K)	IFF $CY_P = 1$
	$B + (A \times 2^N) \longrightarrow B$	& CY → DAR(K)	IFF $CY_P = 0$ [5]
LDA CND()[2]	$(A \times 2^N) \longrightarrow B$		IFF DAR(K) = 1
	$B \longrightarrow B$		IFF DAR(K) = 0
ABA CND()[8]	$(A \times 2^N) + B \longrightarrow B$		
XOR CND()[8]	$(A \times 2^N) \oplus B \longrightarrow B$		
Analog Instructions			
IN(K)	Signal Sample from Input Channel K		
OUT(K)	D/A to Output Channel K		
CVTS	Determine Sign Bit		
CVT(K)	Perform A/D on Bit K		
EOP	Program Counter to Zero[6]		
NOP	No Operation		
CND(K)	Select Bit K for Conditional Instructions		
CNDS	Select Sign Bit for Conditional Instructions		

Notes:
1. Note that scaling of A always occurs before executing the digital operation.
2. CND() can be either CND(K) or CNDS testing amplitude bits or the sign bit of the DAR respectively.
3. Clarification of CY_{OUT} sense for certain operations. For LDA, XOR, AND, ABS: $CY_{OUT} \rightarrow 0$.
4. B is set to full scale (F.S.) amplitude with the same sign as the "A" port operand.
5. The previous carry bit (CY_P) is tested to determine the operation. The present carry bit (CY) is loaded into the Kth bit location of the DAR. "Present carry (CY) is generated independent of overflow. It will represent the carry (CY) of a calculated 28-bit result."
6. EOP will also enable overflow correction if it was disabled during a program pass. The EOP must occur in ROM location 188.
7. For SUB CNDS operation $\overline{CY} \rightarrow$ DAR(S).
8. Does not affect DAR. In this case, CND is used with XOR/ABA to enable/disable the ALU overflow saturation algorithm. Use of either instruction causes the ALU output to roll over rather than go to full scale with sign bit preserved. An EOP instruction will also enable the ALU overflow sturation algorithm.

TABLE 3.2. CONSTANT MNEMONICS

Mnemonic	Value	Bit Sequence
KP0	0.000	0.000
KP1	0.125	0.001
KP2	0.25	0.010
KP3	0.375	0.011
KP4	0.5	0.100
KP5	0.625	0.101
KP6	0.75	0.110
KP7	0.875	0.111
KM1	−0.125	1.111
KM2	−0.25	1.110
KM3	−0.375	1.101
KM4	−0.5	1.100
KM5	−0.625	1.011
KM6	−0.75	1.010
KM7	−0.875	1.001
KM8	−1.0	1.000

The 2920 Assembler accepts these mnemonics as inputs to specify the 4-bit sequences shown in Table 3.2. These constants are stored as read only "RAM" locations in the 2920. The binary point is placed to the right of the most significant bit (MSB). Longer bit patterns may be obtained by shifting and adding several constants. A right shift operation in the 2920 fills the left most bit positions with the sign bit (0 for positive constants, 1 for negative constants). Negative constants are represented in 2's complement notation.

TABLE 3.3. SCALER MNEMONICS

Scaler Mnemonic	Equivalent Multiplier	Scaler Mnemonic	Equivalent Multiplier
L02	$2^2 = 4.0$	R06	$2^{-6} = 0.015625$
L01	$2^1 = 2.0$	R07	$2^{-7} = 0.0078125$
R00	$2^0 = 1.0$	R08	$2^{-8} = 0.00390625$
R01	$2^{-1} = 0.5$	R09	$2^{-9} = 0.001953125$
R02	$2^{-2} = 0.25$	R10	$2^{-10} = 0.0009765625$
R03	$2^{-3} = 0.125$	R11	$2^{-11} = 0.00048828125$
R04	$2^{-4} = 0.0625$	R12	$2^{-12} = 0.000244140625$
R05	$2^{-5} = 0.03125$	R13	$2^{-13} = 0.0001220703125$

4.0 DESCRIPTION OF SPECTRUM ANALYZER

The purpose of this spectrum analyzer is to determine the long term spectral characteristics of a signal in the 200 Hz to 3.2 kHz frequency band. The approach used is to sweep the input signal through a high resolution (narrowband) bandpass filter and observe the filter response as a function of the frequency sweep. First the spectrum analyzer block diagram and parameters are determined. Then sampled data considerations are taken into account, and finally the 2920 signal processor code is developed in Section 5.0.

4.1 Specifications

A spectrum analyzer which covers the audio frequency range of 200 Hz to 3.2 kHz was selected for this design. The specifications of the analyzer are given in Table 4.1.

TABLE 4.1 SPECTRUM ANALYZER SPECIFICATIONS

- INPUT BANDWIDTH: 3 kHz
- RESOLUTION BANDWIDTH: 100 Hz
- SWEEP RATE: 6 kHz/sec or 0.5 sec/Band
- DYNAMIC RANGE: 48 dB
- INPUTS — ANALOG SIGNAL: $-1V \leq SIG \leq 1V$
- OUTPUTS — FREQUENCY RESPONSE LINEAR AMPLITUDE (VERTICAL AXIS)
 - — FREQUENCY RESPONSE LOG AMPLITUDE (VERTICAL AXIS)
 - — SWEEP WAVEFORM (SAWTOOTH) (HORIZONTAL AXIS)
- OPTIONAL OUTPUTS — VCO (SWEEPING SINUSOID)

4.2 Block Diagram Description

Ideally, a scanning spectrum analyzer could be implemented by simply scanning a tunable narrowband bandpass filter across the input signal band to determine the signal energy at any frequency. Practically speaking it is nearly impossible to design a complex tunable analog filter which can cover a 10 to 1 range of frequencies, especially near DC. Even digital implementations become very complex and hardware inefficient when tuning is required. It is therefore easier to realize the equivalent of the scanning filter by sweeping the signal past a fixed tuned narrowband bandpass filter. This is accomplished by the superheterodyne system illustrated in the block diagram of Figure 4.1.

Additional Functions — The block diagram in Figure 4.1 shows the basic functions or subsystems which must be implemented to operate the spectrum analyzer. In the digital implementation there must also be an input anti-aliasing filter, sample and hold, A/D converter, and the corresponding output D/A converter and reconstruction filter. The analog-digital functions are implemented by a single 2920 signal processor in software.

Block Diagram — The input signal spectrum is first shaped by the input lowpass filter (LPF) (in addition to the anti-aliasing filter shaping) to avoid overlapping spectral components after mixing. The filtered signal then is multiplied (mixed) by the sweeping local oscillator (SLO) to generate upper and lower sidebands centered about the SLO frequency. The spectral characteristics of the system are shown in Figure 4.2. The bandpass filter (BPF) is centered at 4.5 kHz with a 100 Hz bandwidth. Figure 4.2(a) shows the filter characteristics. The SLO sweeps from 1.3 kHz to 4.3 kHz as seen in Figure 4.2(b). After mixing, the upper and lower sidebands are seen in Figures 4.2(c) and (d) for SLO frequencies of 1.3 and 4.3 kHz respectively. Only the upper sideband is of interest however as it is swept across the BPF and the signal energy is extracted. When the SLO is at 1.3 kHz the BPF is looking at the high band (3.2 kHz). As the SLO frequency increases, the apparent signal frequency seen by the BPF decreases until at a SLO frequency of 4.3 kHz, the BPF "sees" the signal energy at 200 Hz (4.5 kHz minus 4.3 kHz).

The block diagram shows that the BPF output is then passed through a full wave rectifier (FWR) and lowpass filter to extract the envelope from the 4.5 kHz carrier which is generated when signal energy is present. The resulting signal spectrum is centered at DC and shown in Figure 4.2(e).

The sweep output provides a horizontal sweep voltage for an X-Y display. The purpose of the delay shown in Figure 4.1 is to synchronize the sweep output with the amplitude response output. This delay should approximately equal the propagation delays of the BPF and output LPF.

I/O — The input to the spectrum analyzer is the analog signal to be analyzed. There are several outputs identified in Figure 4.1. These include the frequency sweep output which becomes the horizontal axis drive to a scope, the VCO output, and the BPF amplitude response (both linear and logarithmic) output which becomes the vertical axis drive to the scope.

4.3. Sampled Data System Considerations

An expansion of the frequency axis in Figure 4.2 to include the sampling frequency at 13 kHz shows the first order aliasing spectra as seen in Figure 4.3. From this figure the limitations and requirements for filter rolloff, bandwidths, and center frequencies become clearer.

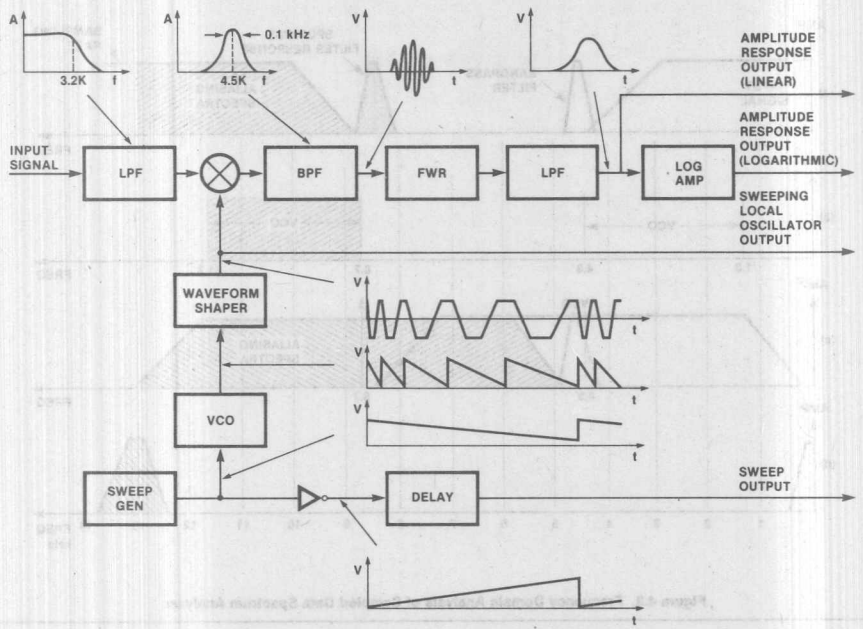


Figure 4.1. Spectrum Analyzer Block Diagram

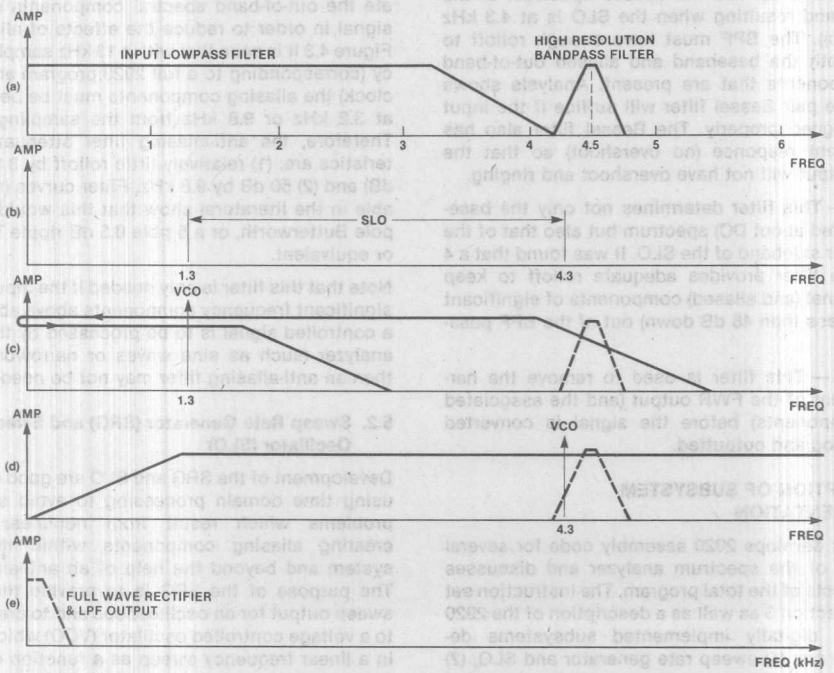


Figure 4.2. Frequency Domain Analysis of Spectrum Analyzer

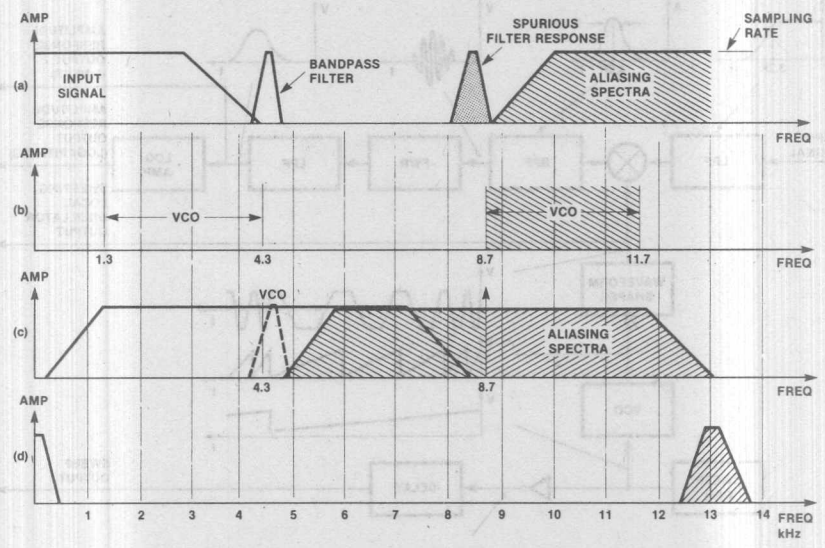


Figure 4.3. Frequency Domain Analysis of Sampled Data Spectrum Analyzer

Bandpass Filter — The location of the bandpass filter is determined by the input lowpass filter bandwidth and rolloff (Figure 4.3(a)) and the aliased spectrum of the lower sideband resulting when the SLO is at 4.3 kHz (Figure 4.3(c)). The BPF must have enough rolloff to eliminate both the baseband and aliased out-of-band signal components that are present. Analysis shows that a 3 pole pair Bessel filter will suffice if the input LPF is designed properly. The Bessel filter also has ideal transient response (no overshoot) so that the resulting output will not have overshoot and ringing.

Input LPF — This filter determines not only the baseband (centered about DC) spectrum but also that of the aliased lower sideband of the SLO. It was found that a 4 pole, 2 zero filter provides adequate rolloff to keep spurious signal (and aliased) components of significant amplitude (less than 48 dB down) out of the BPF passband.

Output LPF — This filter is used to remove the harmonic content of the FWR output (and the associated aliased components) before the signal is converted back to analog and outputted.

5.0 DESCRIPTION OF SUBSYSTEM IMPLEMENTATION

This section develops 2920 assembly code for several subsystems of the spectrum analyzer and discusses various aspects of the total program. The instruction set is given in Section 3 as well as a description of the 2920 device. The digitally implemented subsystems described here are: (1) sweep rate generator and SLO, (2) multiplier, (3) output lowpass filter, and (4) log amplifier. These are discussed following a discussion of the input anti-aliasing filter.

5.1 Anti-aliasing Filter

The basic function of the anti-aliasing filter is to attenuate the out-of-band spectral components of the input signal in order to reduce the effects of aliasing. From Figure 4.3 it is seen that with a 13 kHz sampling frequency (corresponding to a full 2920 program and a 10 MHz clock) the aliasing components must be below −50 dB at 3.2 kHz or 9.8 kHz from the sampling frequency. Therefore, the anti-aliasing filter attenuation characteristics are: (1) relatively little rolloff by 3.2 kHz (say 1 dB) and (2) 50 dB by 9.8 kHz. Filter curves (readily available in the literature) show that this would require a 6 pole Butterworth, or a 5 pole 0.5 dB ripple Tchebyshev, or equivalent.

Note that this filter is only needed if the input signal has significant frequency components above about 7 kHz. If a controlled signal is to be processed by the spectrum analyzer (such as sine waves or narrowband signals) then an anti-aliasing filter may not be needed.

5.2. Sweep Rate Generator (SRG) and Sweeping Local Oscillator (SLO)

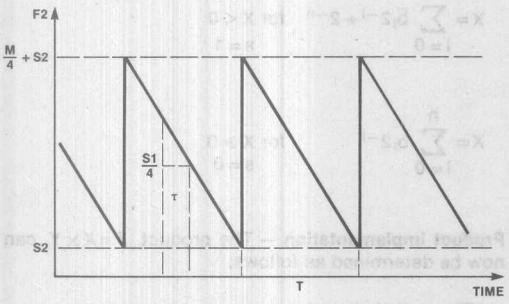
Development of the SRG and SLO are good examples of using time domain processing to avoid some of the problems which result from nonlinear processes creating aliasing components within the sampled system and beyond the help of an anti-aliasing filter. The purpose of the SRG is to provide the horizontal sweep output for an oscilloscope and to create an input to a voltage controlled oscillator (VCO) which will result in a linear frequency sweep as a function of time. The SLO is then a combination of the SRG and VCO, e.g. the sawtooth wave of the SRG drives the VCO resulting in a linear sweeping local oscillator which sweeps between

predetermined frequencies (1.3 kHz and 4.3 kHz) with a sweep rate determined by the period of the sawtooth wave.

Sweep Rate Generator — A sawtooth wave with an offset is the required output of this subsystem. The slope of the sawtooth determines the rate of change of frequency of the VCO, the voltage excursion is proportional to the frequency range of the VCO, and the offset represents the minimum frequency. As an output signal, the sawtooth provides a linear sweep for the horizontal axis of a scope (X-Y display) which is synchronized with the frequency sweep of the VCO. Based on the input specifications, a repetition rate of 2 sweeps/sec is needed.

The sawtooth wave is simply generated by continuously decrementing a register with a fixed value and thereby generating a linear negative slope. When the voltage changes sign (crosses zero) a constant equal to the sawtooth peak amplitude is added. This is accomplished by using an add (ADD) instruction conditioned on the sign bit. Once the sawtooth waveform is generated, it is scaled and a constant offset is added to provide a minimum voltage corresponding to the minimum frequency of the VCO. The resulting waveform and the 2920 program to generate this function is shown in Figure 5.1. Because of the low frequency of this signal (2.0 Hz) compared to the sampling frequency (13 kHz), all aliasing components are negligible. Therefore no action is needed to control them.

The program of Figure 5.1 presupposes the existence of two constants S1 and S2. These constants must be generated by the program prior to their use. Since each constant represents a sequence of ones and zeros, they can be generated several ways. One is to use a combination of shifts and adds of the constants KPx or KMx (see Section 3) to the register S1 or S2. Another approach is to read in a value from outside the chip by performing an A/D conversion of a DC voltage. This would allow both the sweep rate and the frequency range to be controlled externally. Figure 5.2 gives an example of creating the constant S1.



OP	DEST	SOURCE	SHF	COND	COMMENTS
SUB	F1	S1	R00	—	DECREMENT REGISTER
LDA	DAR	F1	R00	—	LOAD DAR
ADD	F1	M	R00	CNDS	CONDITIONED ADD
LDA	F2	F1	R02	—	$F_2 = F_1$ (SCALED)
ADD	F2	S2	R00	—	ADD OFFSET

Figure 5.1. VCO Input Waveform and 2920 Program Example

ASSUME FROM FIGURE 5.1 THAT

$\tau = 76.8\ \mu sec$
M = 1.0 VOLT
T = 0.5 sec

THEN $S1 = \frac{M}{(T/\tau)} = 15.36 \times 10^{-5} \frac{VOLTS}{STEP}$

CONVERTING TO BINARY YIELDS

$$S1 = 15.36 \times 10^{-5} = 2^{-13} + 2^{-15} + 2^{-20}$$
$$= (2^{-1} + 2^{-3} + 2^{-8})2^{-12}$$
$$= (0.10100001)2^{-12}$$

WE SEE THAT BY SPLITTING THE BINARY WORD INTO GROUPS OF 4 BITS YIELDS

$$S1 = \left[\boxed{0.101} + \boxed{0.001}\,2^{-5}\right]2^{-12}$$

FROM SECTION 3.0 TABLE 3.2 THIS EQUALS $[KP5 + KP1 \times 2^{-5}] \times 2^{-12}$ OR IN 2920 ASSEMBLY LANGUAGE

OP	DEST	SOURCE	SHF	COND
LDA	S1	KP5	R00	—
ADD	S1	KP1	R05	—
LDA	S1	S1	R12	—

LESS THAN ONE PERCENT ERROR IN THE SWEEP RATE IS INTRODUCED BY NEGLECTING KP1 R05. THEREFORE, 2 PROGRAM STEPS CAN BE SAVED AND THE CONSTANT CAN BE GENERATED WITH A SINGLE INSTRUCTION

LDA S1 KP5 R12

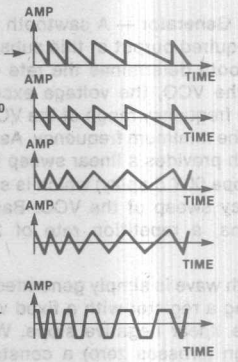
Figure 5.2. Developing the Constant S1 in the 2920

Voltage Controlled Oscillator — The VCO is developed in the same way as the SRG except that the decrement value is not a constant but rather is determined by a scaled version of the SRG input waveform. The calculation would be the same as shown in Figure 5.2 for both ends of the VCO frequency range. An offset would be determined by the low frequency and the scaling factor by the high frequency. The net result would be a sawtooth wave with a varying period as a function of time.

This high frequency sawtooth wave (1.3 kHz to 4.3 kHz) has significant harmonic content which will be reflected by the sampling frequency harmonics and cause distortion of the desired input to the mixer. Digital filters cannot be used here because they are susceptible to the aliasing components also. Some means must therefore be found to reduce the harmonic content of this signal. One approach would be to filter the VCO output using an external filter. This would involve additional hardware plus many extra instructions for I/O and A/D conversion. An alternative is to shape the waveform in the time domain to look more like the desired sinusoid.

By investigating the Fourier Transforms of various symmetric waveforms it is noticed that a trapezoidal waveform can be adjusted so that even harmonics are eliminated and the first odd harmonic is the fifth. This is done by selecting the top of the trapezoid to be 2/3 of the peak of a corresponding triangle wave. The program to accomplish this transformation is shown in Figure 5.3.

	OP	DEST	SOURCE	SHF	COND	COMMENTS
SLO	SUB	OSC1	F2	R00	—	
	LDA	DAR	OSC1	R00	—	
	ADD	OSC1	M	R00	CNDS	
	LDA	OSC	OSC1	R00	—	
WAVEFORM SHAPING	SUB	OSC	M	R01	—	CENTER WAVEFORM ABOUT 0
	ABS	OSC	OSC	L01	—	DOUBLE & TAKE ABS VALUE
	SUB	OSC	M	R01	—	RECENTER ABOUT 0
	ADD	OSC	OSC	L01	—	MULTIPLY BY 3. IF WE SET M = 1 THEN WAVEFORM WILL TRY TO REACH 1.5 AND WILL LIMIT AT 1 (60°) WHICH MINIMIZES 3RD HARMONICS



DEFINITIONS

F1	= SAWTOOTH WAVE VOLTAGE = SOURCE OF VARIABLE STEP SIZE TO SLO
M	= CONSTANT VALUE ≤ 1.0
S2	= MINIMUM STEP SIZE FOR SLO
F2	= F1/4 + S2 = SLO STEP SIZE
OSC1	= BASIC SLO OUTPUT BUT WITH VARIABLE FREQ SAWTOOTH WAVE
OSC	= FINAL SLO OUTPUT AFTER WAVESHAPING
SWEEP RATE	$= \frac{S2}{T} \leq$ RATE $\leq \frac{M/4 + S2}{T}$
T	= SAMPLE PERIOD

Figure 5.3. Sweeping Local Oscillator (SLO) Program

5.3 Implementation of a 4 Quadrant Multiplier

The mixer shown in Figure 4.1 which multiplies the filtered input signal times the SLO waveform must be implemented as a 4 quadrant multiply since both waveforms have positive and negative values. A microprocessor implementation of this multiply might use a shift and add algorithm to determine the magnitude of the product and separate logic to determine the sign. A more direct algorithm is used in the 2920 to avoid the necessity of dealing with the sign bit separately.

Number Representation — It is convenient to form a representation of a number in 2's complement notation since this notation is hardware efficient and is used in the 2920. Assume that X is the multiplier number (sign and magnitude) and Y is the multiplicand. We can represent X in 2's complement as

$$X = (-1)s + s\sum_{i=0}^{n} \bar{b}_i 2^{-i} + \bar{s}\sum_{i=0}^{n} b_i 2^{-i} + s2^{-n}$$

$$= s\left[-1 + \sum_{i=0}^{n} \bar{b}_i 2^{-i} + 2^{-n}\right] + \bar{s}\sum_{i=0}^{n} b_i 2^{-i}$$

where s is the sign bit; 0 is positive, 1 is negative
b_i is the weighting and is either 1 or 0

This can be rewritten as

$$X = -s + x$$

where x represents the magnitude of the amplitude bits excluding the sign bit.

$$X = \sum_{i=0}^{n} \bar{b}_i 2^{-i} + 2^{-n} \quad \text{for } X < 0, \; s = 1$$

$$X = \sum_{i=0}^{n} b_i 2^{-i} \quad \text{for } X \geq 0, \; s = 0$$

Product Implementation — The product, $Z = X \times Y$, can now be determined as follows:

LET $X = (s,x) = -s + x$
$Y = (t,y) = -t + y$

WHERE s = SIGN BIT OF X
t = SIGN BIT OF Y
x = MAGNITUDE OF X
y = MAGNITUDE OF Y

THEN $Z = X \cdot Y$
$= (-s + x)(-t + y)$
$= st + xy - sy - tx$

Now the 2920 can easily implement the product of a positive multiplier and a bipolar multiplicand using a simple shift and conditional add algorithm. The add is conditioned on the value of the multiplier bit located in the DAR.

IF THE SIGN BIT IS IGNORED IN THE MULTIPLIER, X, THE RESULTING PRODUCT WILL BE

$$Z' = (x)(-t+y)$$

$$= xt + xy$$

THIS EXPRESSION LACKS THE TERMS

$$st - sy = s(-Y)$$

WHICH CAN BE ADDED TO FORM THE ENTIRE PRODUCT $Z = Z' + s(-Y)$ BY PERFORMING A CONDITIONAL ADD OF $-Y$ BASED ON THE VALUE OF "s."

The resulting 2920 Assembly code is shown in Figure 5.4 along with comments.

OP	DEST	SOURCE	SHF	COND	COMMENTS
LDA	DAR	X	R00	—	SET UP DAR FOR CONDITIONAL ADD'S, X IS MULTIPLIER
ADD	Z	Y	R01	CND 7	MULTIPLY Y BY THE MAGNITUDE OF X, THAT IS x WHERE $Z = x(-t+y)$
ADD	Z	Y	R02	CND 6	
ADD	Z	Y	R03	CND 5	
ADD	Z	Y	R04	CND 4	
ADD	Z	Y	R05	CND 3	
ADD	Z	Y	R06	CND 2	
ADD	Z	Y	R07	CND 1	
ADD	Z	Y	R08	CND 0	
SUB	Y	Y	L01	—	DEVELOP $-Y$ $Y \leftarrow Y - 2Y = -Y$
ADD	Z	Y	R00	CNDS	CONDITIONAL ADD OF "$-Y$" IF SIGN OF X IS NEGATIVE
SUB	Y	Y	L01	—	RESTORES ORIGINAL SIGN OF Y IF NEEDED

Figure 5.4. 4 Quadrant Multiply Program

5.4 Design and Implementation of the Output Lowpass Filter

The primary purpose of the output lowpass filter is to eliminate the harmonic content of the full wave rectifier (FWR) output and the corresponding aliased components. The filter passband must be at least half that of the narrowband BPF (preferably wider) and the filter complexity should be minimized to reduce amplitude/phase distortion of the signal and ease implementation.

Design Considerations — The FWR spectral output is shown in Figure 5.5 along with the corresponding time domain waveform assuming quasi-static amplitude variation (relatively little change in amplitude over several 4.5 kHz carrier cycles). The desired signal information is located from DC to 50 Hz. All other signal components should be removed by filtering.

The spectral components illustrated in Figure 5.5 will also be centered about multiples of the sampling frequencies (aliasing noise) and must be considered before selecting a filter. This process is tabulated in Table 5.1 where $\Delta f = |Mf_s - Nf_{FWR}|$, N is the FWR harmonic, M is the sampling frequency harmonic and the Δf amplitude is determined by N from Figure 5.5.

From Table 5.1 it is clear that the 1 kHz component (N = 6, M = 2) is the most critical since it is closest to the filter passband and also requires a full 25 dB of attenuation by the filter. The 4 kHz component (N = 2, M = 1) requiring 46.5 dB must also be considered.

A look at the attenuation characteristics of standard filters shows that both criteria are met with a 2 pole Butterworth filter with a bandwidth of 50 Hz.

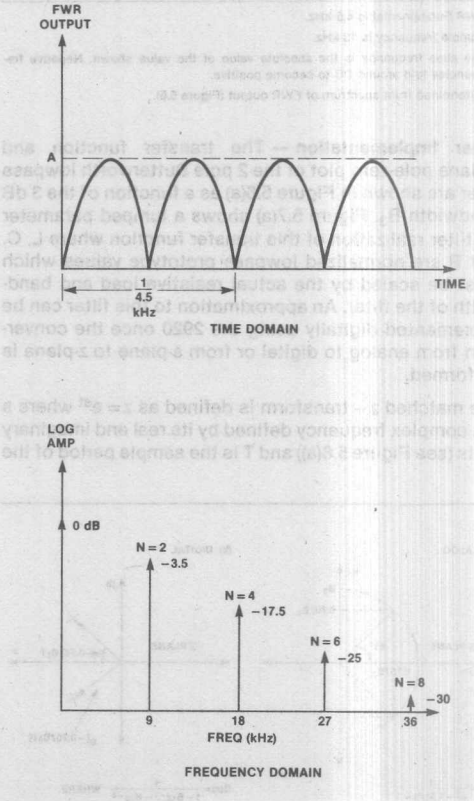


Figure 5.5. Harmonic Analysis of the Full Wave Rectifier (FWR)

TABLE 5.1. ALIASING COMPONENTS OF FWR OUTPUT

FWR[1] HARMONIC N	f_s[2] HARMONIC M	ALIAS[3] FREQ (kHz)	AMPLITUDE[4] LEVEL OF COMPONENT	ATTN REQ'D (to reach 50 dB)
2	1	4	– 3.5 dB	46.5 dB
	2	17		
	3	30		
	4	43		
4	1	– 5	– 17.5 dB	37.5 dB
	2	8		
	3	21		
	4	34		
6	1	– 14	– 25 dB	25 dB
	2	– 1		
	3	12		
	4	25		
8	1	– 23	– 30 dB	20 dB
	2	– 10		
	3	3		
	4	16		
10	1	– 32	– 34 dB	16 dB
	2	– 19		
	3	6		
	4	7		
12	1	– 41	– 37 dB	13 dB
	2	– 28		
	3	– 15		
	4	– 2		

1. FWR Fundamental is 4.5 kHz.
2. Sample frequency is 13 kHz.
3. The alias frequency is the absolute value of the value shown. Negative frequencies fold around DC to become positive.
4. Determined from spectrum of FWR output (Figure 5.5).

Filter Implementation — The transfer function and s-plane pole-zero plot of the 2 pole Butterworth lowpass filter are shown in Figure 5.6(a) as a function of the 3 dB bandwidth B_3. Figure 5.7(a) shows a lumped parameter LC filter realization of this transfer function where L, C, and R are normalized lowpass prototype values which must be scaled by the actual resistive load and bandwidth of the filter. An approximation to this filter can be implemented digitally using the 2920 once the conversion from analog to digital or from s-plane to z-plane is performed.

The matched z – transform is defined as $z = e^{st}$ where s is a complex frequency defined by its real and imaginary parts (see Figure 5.6(a)) and T is the sample period of the sampled data system (the 2920 in this case). Expanding s into its components yields $z = e^{(\sigma T \pm j\omega T)} = e^{\sigma T}\ e^{\pm j\omega T}$ where σ is the real part and ω is the imaginary part of s. This final expression is recognized as a magnitude and a phase which is plotted in Figure 5.6(b) for the 2 pole Butterworth case ($|\sigma| = |j\omega| = 0.707B_3$). The real and imaginary parts of z can now be calculated and the resulting z transform transfer function G(z) determined as seen in Figure 5.6(b).

The transfer function G(z) can be realized digitally with the 2 stage recursive transversal filter shown in Figure 5.7(b) with the feedback coefficients B_1 and B_2 determined from the plot in Figure 5.6(b). The maximum gain through this filter configuration is given by the equation for G_{MAX} (Figure 5.7(b)). Input signal values must be normalized by a gain = $1/G_{MAX}$ or there will be overflows in the filter calculations.

The digital implementation using the 2920 Signal Processor uses RAM locations as the tap points and the transfer of data from one location to another each sample period T as the delay. The tap values (taken from the appropriate memory locations) are then multiplied by the appropriate coefficients using an efficient shift and add software multiply algorithm.

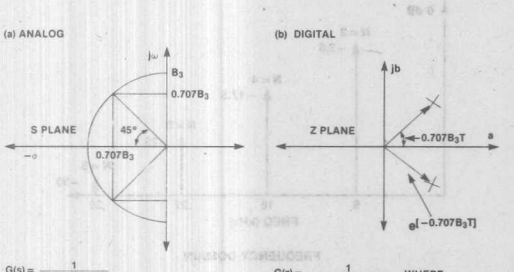


Figure 5.6. LPF Design Filter Transfer Function 2 Pole Butterworth LPF

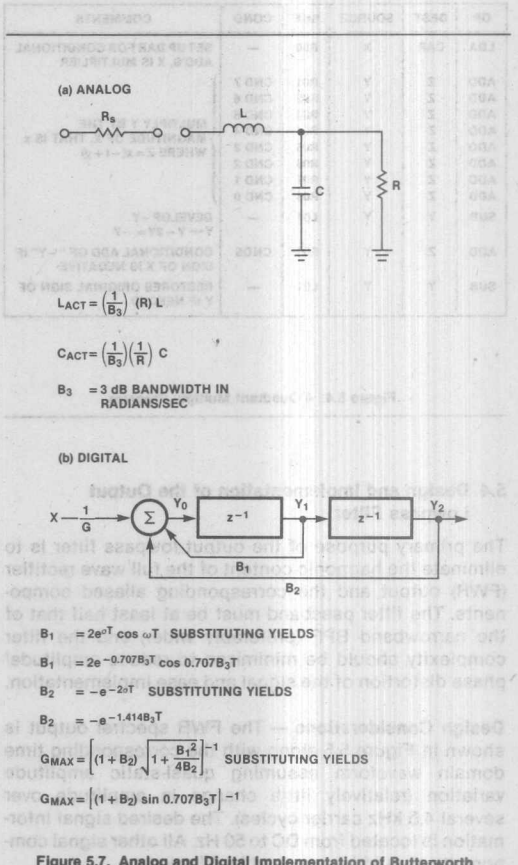


Figure 5.7. Analog and Digital Implementation of Butterworth 2 Pole Lowpass Filter

Filter Calculations — Based on the z-plane plot of poles for the Butterworth filter and the selection of a 50 Hz bandwidth and a 13 kHz sampling frequency, the coefficients of the digital filter can now be implemented. Figure 5.8 shows the calculations leading to both the filter coefficients and the gain weighting factor. The values of B_1 and B_2 after coding should be used to calculate the gain.

COEFFICIENTS

$T = 76.8\ \mu sec\ (f_s = 13\ kHz)$

$B_3 = 2\pi\ (50\ Hz) = 314.16\ rps$

$B_3T = 0.02413$

$B_1 = 1.9659$
$= 01.11110111010000$
$= 2.0 - 2^{-5} - 2^{-9} - 2^{-10}$

$B_2 = -0.966452$
$= -[0.11110111011010]$
$= -[1.0 - 2^{-5} - 2^{-9} - 2^{-12} - 2^{-13}]$

GAIN

$$G_{MAX} = \left[(1 + B_2)\sqrt{1 + \frac{B_1^2}{4B_2}}\right]^{-1}$$

$$= \frac{1}{0.000609}$$

$$= 1640$$

$$G = \frac{1}{G_{MAX}}$$

$$= 0.000609$$

$$> 2^{-11}\ (= 0.000488)$$

Figure 5.8. Digital Filter Calculations

2920 Assembly Language Program — Based on these binary values and their corresponding bit sequences, the lowpass filter can now be implemented digitally using 2920 assembly code. Figure 5.9 shows the program listing and comments which describe what each section of code is accomplishing. The filter variables are shown in Figure 5.7(b).

It can be noted from Figure 5.9 that the feedback of Y2 was begun before the feedback of Y1 was completed. This was done to avoid overflows during the summing of Y0. Although the maximum gain of the filter is known, and has been compensated for, the filter may still overflow during intermediate calculations for certain sequences of instructions.

Also, it should be noted that narrow band filters are very sensitive to coefficient precision. For example, the representation for B_2 required five terms. By omitting only the last term of this coefficient ($Y2 \cdot 2^{-13}$), the cutoff for this filter moves from 53 Hz to 65 Hz.

5.5 Logarithmic Amplifier

The logarithmic amplifier is a function which is usually included as part of a spectrum analyzer. Its purpose is to amplify low level signal components for easier comparison with larger signals. Furthermore, the log amplifier described here provides an example of the use of 2920 code to implement a piecewise linear approximation of a general function. The dynamic range of the amplifier is 50 dB with an error of less than 1 dB for signal levels to −30 dB. The transfer characteristic is shown in Figure 5.10.

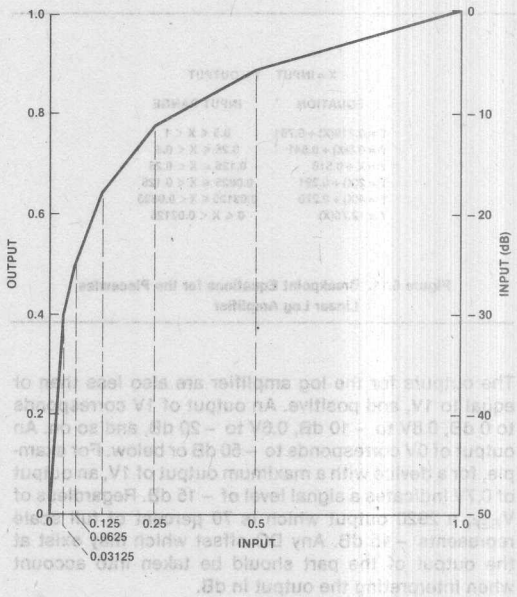


Figure 5.10. Transfer Characteristic of Piecewise Linear Log Amplifier

OP	DEST	SOURCE	SHF	CND	COMMENT
LDA	Y2	Y1	R00	—	PROPAGATES SAMPLES THROUGH DELAY LINE
LDA	Y1	Y0	R00	—	
SUB	Y0	Y1	R05	—	$1 - 2^{-5}$ (Y0 STILL CONTAINS Y1)
SUB	Y0	Y1	R09	—	FEEDBACK $B_1 Y_1$ TO Y0 WHERE $B_1 = 2.0 - 2^{-5} - 2^{-9} - 2^{-10}$
SUB	Y0	Y1	R10	—	
SUB	Y0	Y2	R00	—	
ADD	Y0	Y1	R00	—	
ADD	Y0	Y2	R05	—	FEEDBACK $B_2 Y_2$ TO Y0 WHERE $B_2 = -[1.0 - 2^{-5} - 2^{-9} - 2^{-12} - 2^{-13}]$
ADD	Y0	Y2	R09	—	
ADD	Y0	Y2	R12	—	
ADD	Y0	Y2	R13	—	
ADD	Y0	X	R11	—	ADJUST X BY GAIN $G = 2^{-11}$
LDA	DAR	Y0	R00	—	LOAD FILTER OUTPUT TO DAR FOR OUTPUTTING FROM 2920

Figure 5.9. Program for Digital Implementation of 2 Pole Butterworth Lowpass Filter

Six linear sections are used to approximate the log amplifier. The equations for these sections and the range of inputs for which each equation is used are given in Figure 5.11. The equations were obtained graphically, and then adjusted for coding efficiency. The input for the log amplifier must be positive and less than or equal to 1V. To simplify matters, the endpoints for the linear sections were chosen as powers of two. This way, only one bit of the number to be processed need be checked to determine whether that number falls within an input range. The constant multipliers (slopes) of the linear sections were chosen to minimize error while at the same time allowing the multiplications to be efficiently handled in 2920 code.

X = INPUT Y = OUTPUT

EQUATION	INPUT RANGE
$Y = 0.219(X) + 0.781$	$0.5 \leq X < 1$
$Y = 0.5(X) + 0.641$	$0.25 \leq X < 0.5$
$Y = X + 0.516$	$0.125 \leq X < 0.25$
$Y = 2(X) + 0.391$	$0.0625 \leq X < 0.125$
$Y = 4(X) + 0.270$	$0.03125 \leq X < 0.0625$
$Y = 12.75(X)$	$0 \leq X < 0.03125$

Figure 5.11. Breakpoint Equations for the Piecewise Linear Log Amplifier

The outputs for the log amplifier are also less than or equal to 1V, and positive. An output of 1V corresponds to 0 dB, 0.8V to −10 dB, 0.6V to −20 dB, and so on. An output of 0V corresponds to −50 dB or below. For example, for a device with a maximum output of 1V, an output of 0.7V indicates a signal level of −15 dB. Regardless of V_{REF}, a 2920 output which is 70 percent of full scale represents −15 dB. Any DC offset which may exist at the output of the part should be taken into account when interpreting the output in dB.

A flow chart of the log amplifier program is shown in Figure 5.12, and the assembly code is given in Figure 5.13. The first linear section of the amplifier to be implemented is the sixth section, which corresponds to inputs less than 1/32V. However, all input signals, regardless of amplitude, are processed by the equation for this section initially. The original signal is then placed in the DAR. All the following operations are conditional, and are performed only if the tested bit of the DAR is a "one." Otherwise, a NOP is performed. Each bit of the DAR is tested, starting with the least significant bit, until a "one" is found. Once a "one" is located, the multiplier and offset corresponding to the indicated range of the input are used to compute the result. This result replaces any previously computed result. If no "ones" are encountered, the input is less than 1/32V, and only NOP's are performed. The value computed for the sixth section then remains unmodified. Since the program starts checking for small signals and progresses to large signals, the computed value which corresponds to the signal range into which the input signal falls will be the final result.

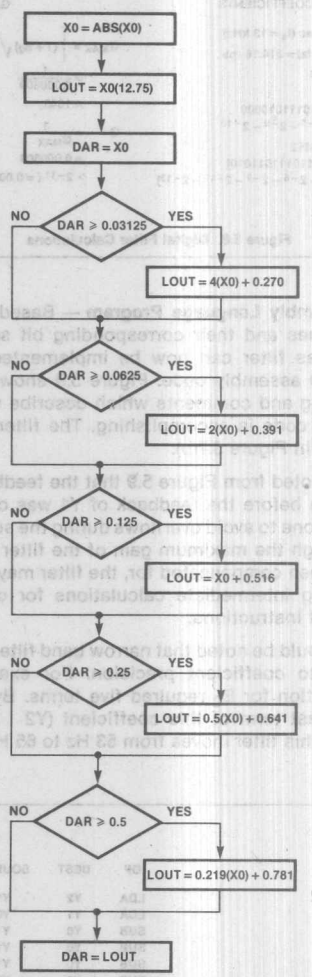


Figure 5.12. Flowchart for Implementation of Piecewise Linear Log Amplifier

```
***LOG AMP*****

ABS YO,YO,R00                    ;PREVENT PROCESSING OF NEGATIVE NUMBERS

;   SECTION 6

LDA LOUT,YO,L02                  ;LOUT = 12.75(XO)   ,   0 < XO < 0.03125
ADD LOUT,YO,L02
ADD LOUT,YO,L02
ADD LOUT,YO,R01
ADD LOUT,YO,R02

LDA DAR,YO,R00                   ;TRANSFER INPUT TO DAR TO DO CONDITIONAL ARITHMETIC

;   SECTION 5

LDA LOUT,YO,L02,CND3             ;LOUT = 4(XO) + 0.270   ,   0.03125 < XO < 0.0625
ADD LOUT,KP2,R00,CND3
ADD LOUT,KP5,R05,CND3

;   SECTION 4

LDA LOUT,YO,L01,CND4             ;LOUT = 2(XO) + 0.391   ,   0.0625 < XO < 0.125
ADD LOUT,KP3,R00,CND4
ADD LOUT,KP2,R04,CND4

;   SECTION 3

LDA LOUT,YO,R00,CND5             ;LOUT = XO + 0.516   ,   0.125 < XO < 0.25
ADD LOUT,KP4,R00,CND5
ADD LOUT,KP2,R04,CND5

;   SECTION 2

LDA LOUT,YO,R01,CND6             ;LOUT = 0.5(XO) + 0.641   ,   0.25 < XO < 0.5
ADD LOUT,KP5,R00,CND6
ADD LOUT,KP2,R04,CND6

;   SECTION 1

LDA LOUT,YO,R03,CND7             ;LOUT = 0.219(XO) + 0.781   ,   0.5 < XO < 1
ADD LOUT,YO,R04,CND7
ADD LOUT,YO,R05,CND7
ADD LOUT,KP6,R00,CND7
ADD LOUT,KP4,R04,CND7

LDA DAR,LOUT,R00                 ;TRANSFER RESULT TO DAR TO OUTPUT OR OTHER
                                 ;REGISTER FOR FURTHER PROCESSING
```

Figure 5.13. Log Amplifier Assembly Code

6.0 SUMMARY

The examples given in Section 5 illustrate some of the design techniques used when implementing an analog function with the 2920 signal processor. The complete spectrum analyzer program listing is given in Appendix A. This listing contains subsystems which were not given as examples including the input lowpass and bandpass filters. Table 6.1 summarizes the number of instructions needed for each subsystem and the total number of instructions and scratch pad RAM locations needed for this implementation. The object code listing is also given in Appendix A. It contains the actual bit sequences loaded into the EPROM.

SUBSYSTEM	# INSTRUCTIONS
MISCELLANEOUS I/O	19
INPUT LOWPASS FILTER	28
MULTIPLIER	12
SRG	18
VCO	10
BPF	31
FWR + LPF	13
LOG AMPLIFIER	24
TOTAL INSTRUCTIONS	155
# RAM LOCATIONS	25

APPENDIX A. COMPLETE SPECTRUM ANALYZER ASSEMBLY LISTING

The spectrum analyzer program listed in this appendix (Figure A.2) was coded in a structured form, with each functional block coded separately and the blocks arranged to follow the signal paths shown in the block diagram of Figure 4.1. This was done for clarity in describing the program. It is not necessary to implement the code one functional block at a time or in any specific order as long as the relationships between the inputs and outputs of the functional blocks remains unchanged. In fact, it is usually more efficient to program the 2920 in a less structured form. For example, because each functional block is executed in its entirety before proceeding to the next functional block, it was not possible to execute all input and output instructions simultaneously with digital instructions. To take advantage of the fact that analog and digital instructions can execute simultaneously, portions of the program could be rearranged, and these analog instructions combined with digital instructions, thus reducing the program length.

The first functional block of the spectrum analyzer program is the 4 pole, 2 zero input filter. The sections titled Pole 1 and Pole 3 each represent a complex pole pair. The filter stage propagation is executed after the input signal is obtained. Stage propagation must be done before the complex zero pair can be implemented.

After the input filter program, the sweep waveform is generated to drive the VCO. This waveform is also inverted and delayed to form the horizontal output of the spectrum analyzer. The delay of 10 msec with respect to the VCO input compensates for the propagation delay of the bandpass and output filters. This delay is implemented in the time domain by simply subtracting a constant from the sawtooth waveform which corresponds to the change in amplitude of the waveform during a 10 ms period of time. The two NOP's which appear in the sweep oscillator sequence are part of the output sequence and are used to settle the D/A converter.

The VCO is implemented next. The sweeping sawtooth is set to zero at the beginning of each sweep so that the VCO output can be more easily observed with an oscilloscope. Once both the VCO waveform and the input signal have been obtained, they are multiplied together using the four quadrant multiply algorithm. With regard to Figure 5.4, OSC = X, MPL2 = Y, and MPL1 = Z.

The signal from the multiplier (mixer) is then passed to the 6 pole bandpass filter. Portions of the output sequences for the VCO and linear and log response outputs are also executed at this time. Executing these sequences simultaneously with the digital instructions saves program steps.

The signal is then processed by the full wave rectifier and output lowpass filter. (Referring back to Figure 5.9, BP50 corresponds to the input X. Also, in step 129, the right shift 11 of Figure 5.9 was replaced with a right shift 9. Since the output of the BPF is not full scale, less gain compensation is needed.) The output of this filter is the linear amplitude response of the spectrum analyzer. The log amplifier is the final section of the program, and provides a log amplitude response output. All unused program steps are NOP's. The symbol table used by the assembler is shown in Figure A.1, and a listing of the spectrum analyzer object code is given in Figure A.3.

Acknowledgement — The authors would like to thank Wallace Li for the work he did in developing the initial spectrum analyzer program and demonstrating its operation in a 2920.

SYMBOL:	VALUE:
TEMP	0
IF11	1
IF10	2
IF31	3
IF30	4
MPL2	5
S1	6
M	7
F1	8
SWP	9
F2	10
S2	11
OSC1	12
OSC	13
MPL1	14
BP11	15
BP10	16
BP31	17
BP30	18
YO	19
BP51	20
BP50	21
LOUT	22
Y2	23
Y1	24

Figure A-1. Spectrum Analyzer Symbol Table

```
ISIS-II 2920 ASSEMBLER X102                                    PAGE   1

ASSEMBLER INVOKED BY:  AS2920 SPEC4 DEBUG


 LINE  LOC OBJECT SOURCE STATEMENT

    1    0 3066EB SUB DAR,   DAR,   R00,  IN3      ;CLEAR DAR FOR A/D CONVERSION
    2    1 3000EF IN3
    3    2 3000EF IN3
    4    3 3000EF IN3
    5    4 3000EF IN3
    6    5 3000EF IN3
    7    6 4000EF NOP
    8    7 4000EF NOP
    9    8 6000EF CVTS
   10    9 EBE6ED ADD DAR,   KM2,   R00,  CND6     ;A/D CONVERSION INSTRUCTION
   11   10 4000EF NOP
   12   11 4000EF NOP
   13   12 7100EF CVT7
   14   13 4000EF NOP
   15
   16              ;*****INPUT FILTER*****
   17
   18              ;POLE 1
   19   14 4008EF LDA TEMP,  IF11,  R00,  NOP
   20   15 6300FF LDA IF11,  IF10,  R00,  CVT6
   21   16 46002A SUB IF10,  IF10,  R02,  NOP
   22   17 4600AA SUB IF10,  IF10,  R06,  NOP
   23   18 57000D ADD IF10,  IF10,  R09,  CVT5
   24   19 44002A SUB IF10,  TEMP,  R02,  NOP
   25   20 4400AC ADD IF10,  TEMP,  R06,  NOP
   26   21 45000D ADD IF10,  TEMP,  R09,  CVT4
   27   22 44002D ADD IF10,  TEMP,  R10,  NOP
   28   23 44006B SUB IF10,  TEMP,  R12,  NOP
   29
   30              ;POLE 3
   31   24 3308EF LDA TEMP,  IF31,  R00,  CVT3
   32   25 4C00FF LDA IF31,  IF30,  R00,  NOP
   33   26 40100F LDA IF30,  TEMP,  R09,  NOP
   34   27 21100A SUB IF30,  TEMP,  R01,  CVT2
   35   28 40104A SUB IF30,  TEMP,  R03,  NOP
   36   29 48106C ADD IF30,  IF30,  R04,  NOP
   37   30 13184C ADD IF30,  IF31,  R03,  CVT1
   38   31 42188A SUB IF30,  IF31,  R05,  NOP
   39   32 4218CC ADD IF30,  IF31,  R07,  NOP
   40   33 03182D ADD IF30,  IF31,  R10,  CVT0
   41
   42              ;STAGE PROPAGATION
   43   34 44224C ADD IF10,  DAR,   R03           ;ADD INPUT TO INPUT FILTER
   44   35 4210ED ADD IF30,  IF10,  R00           ;GAIN=4.21/2**3
   45
   46              ;ZERO 5
   47   36 4810FF LDA MPL2,  IF30,  R00
   48   37 4218FD ADD MPL2,  IF31,  R00
   49   38 42185C ADD MPL2,  IF31,  R03
   50   39 4218FC ADD MPL2,  IF31,  R08
   51   40 42181D ADD MPL2,  IF31,  R09
   52   41 4010FD ADD MPL2,  TEMP,  R00           ;INPUT FILTER OUTPUT IN MPL2
```

Figure A.2. Complete Spectrum Analyzer Assembly Listing

```
LINE  LOC OBJECT SOURCE STATEMENT

  53
  54
  55                    ;*****SWEEP OSC*****
  56
  57
  58    42 4C9A6F LDA S1,    KP5,  R12           ;DEFINE S1
  59    43 4C92DF LDA M,     KP4,  L01           ;DEFINE M
  60    44 4A40EB SUB F1,    S1,   R00
  61    45 4064EF LDA DAR,   F1,   R00
  62    46 7A48ED ADD F1,    M,    R00, CNDS
  63    47 4ACAF5 LIM SWP,   KP7,  R00
  64    48 4060FB SUB SWP,   F1,   R00           ;INVERT SLOPE
  65    49 406CEF LDA DAR,   SWP,  R00           ;SWEEP TO DAR TO OUTPUT
  66    50 48CE8A SUB DAR,   KP5,  R05
  67    51 78C6CD ADD DAR,   KP4,  L01, CNDS     ;10 MS DELAY FOR FILTER RISE TIMES
  68    52 44602E LDA F2,    F1,   R02, NOP      ;SAWTOOTH SCALING
  69    53 4460AA SUB F2,    F1,   R06, NOP
  70    54 46606B SUB F2,    F2,   R12, NOP
  71    55 4460EA SUB F2,    F1,   R08, NOP
  72    56 4000EF NOP
  73    57 4000EF NOP
  74    58 86CA3E LDA S2,    KP3,  R02, OUT0     ;DEFINE S2
  75    59 86CABC ADD S2,    KP3,  R06, OUT0
  76    60 84CA1D ADD S2,    KP1,  R09, OUT0
  77    61 8668ED ADD F2,    S2,   R00, OUT0     ;ADD OFFSET
  78
  79
  80                    ;*****VCO*****
  81
  82
  83    62 8000EF OUT0
  84    63 8270EB SUB OSC1,  F2,   R00, OUT0
  85    64 4864EF LDA DAR,   OSC1, R00
  86    65 7A58ED ADD OSC1,  M,    R00, CNDS
  87    66 4870FF LDA OSC,   OSC1, R00
  88    67 4A581A SUB OSC,   M,    R01
  89    68 4878D7 ABS OSC,   OSC,  L01
  90    69 4A581A SUB OSC,   M,    R01
  91    70 4064EF LDA DAR,   F1,   R00
  92    71 70D2EF LDA OSC1,  KP0,  R00, CNDS     ;SET VCO TO 0 TO SYNC WITH SWEEP
  93    72 4878DD ADD OSC,   OSC,  L01           ;VCO OUTPUT IN OSC
  94
  95
  96                    ;******MULTIPLY*****
  97
  98
  99    73 4E70EB SUB MPL1,  MPL1, R00           ;CLEAR MULTIPLY OUTPUT REGISTER
 100    74 486CEF LDA DAR,   OSC,  R00           ;LOAD DAR WITH MULTIPLIER
 101    75 FD580C ADD MPL1,  MPL2, R01, CND7
 102    76 ED582C ADD MPL1,  MPL2, R02, CND6
 103    77 DD584C ADD MPL1,  MPL2, R03, CND5
 104    78 CD586C ADD MPL1,  MPL2, R04, CND4
 105    79 BD588C ADD MPL1,  MPL2, R05, CND3
 106    80 AD58AC ADD MPL1,  MPL2, R06, CND2
```

Figure A.2. Complete Spectrum Analyzer Assembly Listing (cont'd)

```
 LINE  LOC OBJECT SOURCE STATEMENT

  107   81 9D58CC ADD MPL1, MPL2, R07, CND1
  108   82 8D58EC ADD MPL1, MPL2, R08, CND0
  109   83 4818DB SUB MPL2, MPL2, L01        ;DEVELOP -Y
  110   84 7C58ED ADD MPL1, MPL2, R00, CNDS  ;ADD -Y IF MULTIPLIER IS NEGATIVE
  111
  112
  113              ;*****BAND-PASS FILTER*****
  114
  115
  116              ;POLE 1
  117   85 4A28EF LDA TEMP, BP11, R00, NOP
  118   86 44D0FF LDA BP11, BP10, R00, NOP
  119   87 4A298E LDA BP10, BP11, R05, NOP
  120   88 4A29EB SUB BP10, BP11, R00, NOP
  121   89 40814C ADD BP10, BP10, R03, NOP
  122   90 4081EA SUB BP10, BP10, R08, NOP
  123   91 A001EB SUB BP10, TEMP, R00, OUT2  ;OUTPUT VCO SINE WAVE
  124   92 A0018C ADD BP10, TEMP, R05, OUT2
  125   93 A001CA SUB BP10, TEMP, R07, OUT2
  126
  127              ;POLE 3
  128   94 A088EF LDA TEMP, BP31, R00, OUT2
  129   95 A281FF LDA BP31, BP30, R00, OUT2
  130   96 A401AE LDA BP30, TEMP, R06, OUT2
  131   97 4401EB SUB BP30, TEMP, R00
  132   98 42CCEF LDA DAR,  YO,   R00         ;LINEAR OUTPUT TO DAR
  133   99 4681CA SUB BP30, BP30, R07, NOP
  134  100 4489EB SUB BP30, BP31, R00, NOP
  135  101 44894A SUB BP30, BP31, R03, NOP
  136  102 44898A SUB BP30, BP31, R05, NOP
  137  103 4489CC ADD BP30, BP31, R07, NOP
  138
  139              ;POLE 5
  140  104 4880EF LDA TEMP, BP51, R00, NOP
  141  105 C899EF LDA BP51, BP50, R00, OUT4
  142  106 C0119E LDA BP50, TEMP, R05, OUT4
  143  107 C0113D ADD BP50, TEMP, R10, OUT4
  144  108 C011FB SUB BP50, TEMP, R00, OUT4
  145  109 C899FC ADD BP50, BP50, R08, OUT4
  146  110 C891FB SUB BP50, BP51, R00, OUT4
  147  111 48915A SUB BP50, BP51, R03
  148  112 4AC4EF LDA DAR,  LOUT, R00        ;LOG OUTPUT TO DAR
  149  113 4891BC ADD BP50, BP51, R06, NOP
  150  114 48911B SUB BP50, BP51, R09, NOP
  151
  152              ;STAGE PROPAGATION
  153  115 4A21AC ADD BP10, MPL1, R06, NOP
  154  116 44816C ADD BP30, BP10, R04, NOP
  155  117 42917C ADD BP50, BP30, R04, NOP
  156
  157
  158              ;*****LOW PASS FILTER*****
  159
  160
```

Figure A.2. Complete Spectrum Analyzer Assembly Listing (cont'd)

```
 LINE  LOC OBJECT SOURCE STATEMENT

  161  118 44B1FF LDA Y2,   Y1,   R00, NOP
  162  119 E2C9EF LDA Y1,   Y0,   R00, OUT6
  163  120 E4A19A SUB Y0,   Y1,   R05, OUT6
  164  121 E4A11B SUB Y0,   Y1,   R09, OUT6
  165  122 E4A13B SUB Y0,   Y1,   R10, OUT6
  166  123 EE89FB SUB Y0,   Y2,   R00, OUT6
  167  124 E4A1FD ADD Y0,   Y1,   R00, OUT6
  168  125 4E899C ADD Y0,   Y2,   R05
  169  126 4E891D ADD Y0,   Y2,   R09
  170  127 4E897D ADD Y0,   Y2,   R12
  171  128 4E899D ADD Y0,   Y2,   R13
  172  129 4C8919 ABA Y0,   BP50, R09          ;FULL WAVE RECTIFIER OPERATION
  173  130 4689FF LDA Y0,   Y0,   R00
  174
  175
  176              ;*****LOG AMP*****
  177
  178
  179  131 4689F7 ABS Y0,   Y0,   R00          ;PREVENT PROCESSING OF NEGATIVE NUMBERS
  180  132 4699AF LDA LOUT, Y0,   L02          ;SECTION 6
  181  133 4699AD ADD LOUT, Y0,   L02
  182  134 4699AD ADD LOUT, Y0,   L02
  183  135 46990C ADD LOUT, Y0,   R01
  184  136 46992C ADD LOUT, Y0,   R02
  185  137 42CCEF LDA DAR,  Y0,   R00
  186  138 B799AF LDA LOUT, Y0,   L02, CND3    ;SECTION 5
  187  139 B793ED ADD LOUT, KP2,  R00, CND3
  188  140 BD9B8C ADD LOUT, KP5,  R05, CND3
  189  141 C799CF LDA LOUT, Y0,   L01, CND4    ;SECTION 4
  190  142 C79BED ADD LOUT, KP3,  R00, CND4
  191  143 C7936C ADD LOUT, KP2,  R04, CND4
  192  144 D799EF LDA LOUT, Y0,   R00, CND5    ;SECTION 3
  193  145 DD93ED ADD LOUT, KP4,  R00, CND5
  194  146 D7936C ADD LOUT, KP2,  R04, CND5
  195  147 E7990E LDA LOUT, Y0,   R01, CND6    ;SECTION 2
  196  148 ED9BED ADD LOUT, KP5,  R00, CND6
  197  149 E7936C ADD LOUT, KP2,  R04, CND6
  198  150 F7994E LDA LOUT, Y0,   R03, CND7    ;SECTION 1
  199  151 F7996C ADD LOUT, Y0,   R04, CND7
  200  152 F7998C ADD LOUT, Y0,   R05, CND7
  201  153 FF93ED ADD LOUT, KP6,  R00, CND7
  202  154 FD936C ADD LOUT, KP4,  R04, CND7
  203  155 4000EF NOP
  204  156 4000EF NOP
  205  157 4000EF NOP
  206  158 4000EF NOP
  207  159 4000EF NOP
  208  160 4000EF NOP
  209  161 4000EF NOP
  210  162 4000EF NOP
                •
                •
                •
  236  188 5000EF EOP
  237  189 4000EF NOP
  238  190 4000EF NOP
  239  191 4000EF NOP
  240              END
```

Figure A.2. Complete Spectrum Analyzer Assembly Listing (cont'd)

```
:18000000F3F0F6F6FEFBF3F0F0F0FEFFF3F0F0F0FEFFF3F0F0F0FEFFE0
:18001800F3F0F0F0FEFFF3F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFCE
:18003000F6F0F0F0FEFFFEFBFEF6FEFDF4F0F0F0FEFFF4F0F0F0FEFF8B
:18004800F7F1F0F0FEFFF4F0F0F0FEFFF4F0F0F8FEFFF6F3F0F0FFFF8A
:18006000F4F6F0F0F2FAF4F6F0F0FAFAF5F7F0F0F0FDF4F4F0F0F2FAA7
:18007800F4F4F0F0FAFCF4F5F0F0F0FDF4F4F0F0F2FDF4F4F0F0F6FB8C
:18009000F3F3F0F8FEFFF4FCF0F0FFFFF4F0F1F0F0FFF2F1F1F0F0FA5D
:1800A800F4F0F1F0F4FAF4F8F1F0F6FCF1F3F1F8F4FCF4F2F1F8F8FA50
:1800C000F4F2F1F8FCFCF0F3F1F8F2FDF4F4F2F2F4FCF4F2F1F0FEFD28
:1800D800F4F8F1F0FFFFF4F2F1F8FFFDF4F2F1F8F5FCF4F2F1F8FFFCF0
:1800F000F4F2F1F8F1FDF4F0F1F0FFFDF4FCF9FAF6FFF4FCF9F2FDFFCB
:18010800F4FAF4F0FEFBF4F0F6F4FEFFF7FAF4F8FEFDF4FAFCFAFFF599
:18012000F4F0F6F0FFFBF4F0F6FCFEFFF4F8FCFEF8FAF7F8FCF6FCFD7E
:18013800F4F4F6F0F2FEF4F4F6F0FAFAF4F6F6F0F6FBF4F4F6F0FEFAA8
:18015000F4F0F0F0FEFFF4F0F0F0FEFFF8F6FCFAF3FEF8F6FCFAFBFC65
:18016800F8F4FCFAF1FDF8F6F6F8FEFDF8F0F0F0FEFFF8F2F7F0FEFB49
:18018000F4F8F6F4FEFFF7FAF5F8FEFDF4F8F7F0FFFFF4FAF5F8F1FA24
:18019800F4F8F7F8FDF7F4FAF5F8F1FAF4F0F6F4FEFFF7F0FDF2FEFF1C
:1801B000F4F8F7F8FDFDF4FEF7F0FEFBF4F8F6FCFEFFFFFDF5F8F0FCE0
:1801C800FEFDF5F8F2FCFDFDF5F8F4FCFCFDF5F8F6FCFBFDF5F8F8FCC1
:1801E000FAFDF5F8FAFCF9FDF5F8FCFCF8FDF5F8FEFCF4F8F1F8FDFBA9
:1801F800F7FCF5F8FEFDF4FAF2F8FEFFF4F4FDF0FFFFF4FAF2F9F8FE9D
:18021000F4FAF2F9FEFBF4F0F8F1F4FCF4F0F8F1FEFAFAF0F0F1FEFBBE
:18022800FAF0F0F1F8FCFAF0F0F1FCFAFAF0F8F8FEFFFAF2F8F1FFFF94
:18024000FAF4F0F1FAFEF4F4F0F1FEFBF4F2FCFCFEFFF4F6F8F1FCFA79
:18025800F4F4F8F9FEFBF4F4F8F9F4FAF4F4F8F9F8FAF4F4F8F9FCFC59
:18027000F4F8F8F0FEFFFCF8F9F9FEFFFCF0F1F1F9FEFCF0F1F1F3FD3F
:18028800FCF0F1F1FFFBFCF8F9F9FFFCFCF8F9F1FFFBF4F8F9F1F5FA18
:1802A000F4FAFCF4FEFFF4F8F9F1FBFCF4F8F9F1F1FBF4FAF2F1FAFC15
:1802B800F4F4F8F1F6FCF4F2F9F1F7FCF4F4FBF1FFFFFEF2FCF9FEFFF4
:1802D000FEF4FAF1F9FAFEF4FAF1F1FBFEF4FAF1F3FBFEFEF8F9FFFBCB
:1802E800FEF4FAF1FFFDF4FEF8F9F9FCF4FEF8F9F1FDF4FEF8F9F7FDA5
:18030000F4FEF8F9F9FDF4FCF8F9F1F9F4F6F8F9FFFFF4F6F8F9FFF797
:18031800F4F6F9F9FAFFF4F6F9F9FAFDF4F6F9F9FAFDF4F6F9F9F0FC8A
:18033000F4F6F9F9F2FCF4F2FCFCFEFFFBF7F9F9FAFFFBF7F9F3FEFD5A
:18034800FBFDF9FBF8FCFCF7F9F9FCFFFCF7F9FBFEFDFCF7F9F3F6FC2A
:18036000FDF7F9F9FEFFFDFDF9F3FEFDFDF7F9F3F6FCFEF7F9F9F0FE1A
:18037800FEFDF9FBFEFDFEF7F9F3F6FCFFF7F9F9F4FEFFF7F9F9F6FCFC
:18039000FFF7F9F9F8FCFFFFF9F3FEFDFFFDF9F3F6FCF4F0F0F0FEFFF9
:1803A800F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFF39
:1803C000F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFF21
:1803D800F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFF09
:1803F000F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF1
:18040800F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFD8
:18042000F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFC0
:18043800F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFA8
:18045000F4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFF90
:18046800F5F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFFF4F0F0F0FEFF77
:00000001FF
```

Figure A.3. Spectrum Analyzer Object Code

2920 SOFTWARE SUPPORT PACKAGE

- **Complete software design and development support for the 2920**
- **Extends Intellec® Microcomputer Development System to support 2920 software development**

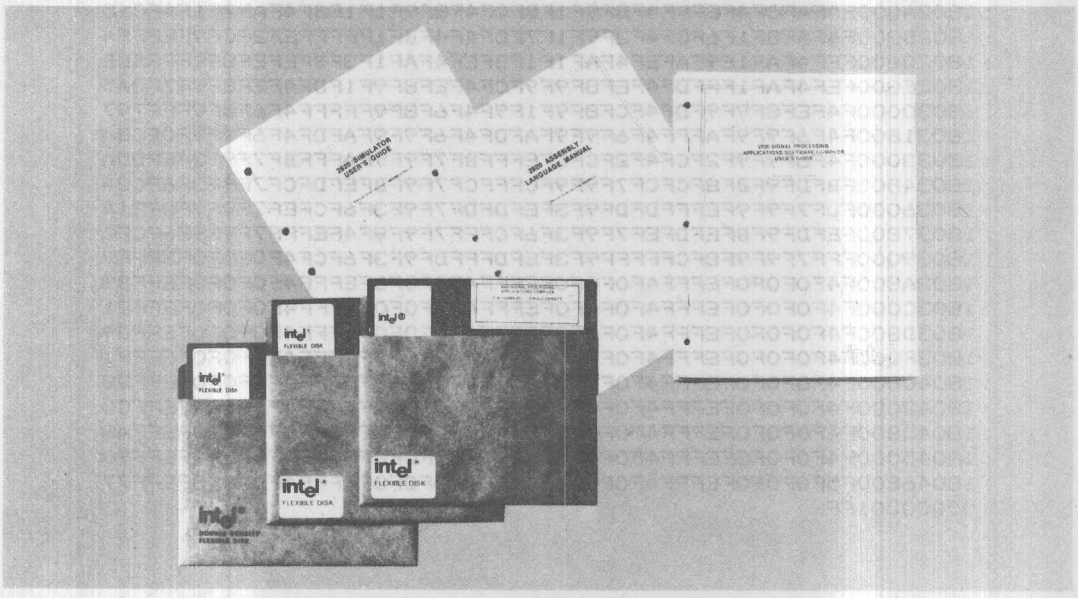
The 2920 Software Support Package furnishes a 2920 Signal Processing Applications Software/Compiler, 2920 Assembler, and 2920 Software Simulator. These three software design and development tools run on the Intellec® Microcomputer Development System.

The 2920 Signal Processing Application Software/Compiler is an interactive tool for designing software to be executed on the 2920 Signal Processor. The compiler accepts English-like statements from the user and generates 2920 assembly language code.

The assembler translates symbolic 2920 assembly language programs into the machine operation code. The user can load the code into the simulator for 2920 simulation or to the Universal PROM Programmer for 2920 EPROM programming.

The simulator, operating entirely in software, allows the user to test and symbolically debug 2920 programs. The user can specify input signals, simulate program execution, set up breakpoints, display input and output, and display and alter the contents of the 2920 registers and memory locations. The simulator can also stop or trace the program and constructively give the user access to the key elements inside a 2920 for analyzing his program.

The compiler, assembler, and simulator enable the designer to develop and test an entire program without a complete prototype design. The 2920 designer works on the Intellec® Microcomputer Development System rather than on a breadboard. The development system can program, store and recall programs or routines and aid in 2920 program design.



2920 Software Support Package

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2920 SIGNAL PROCESSING APPLICATIONS SOFTWARE/COMPILER

- **Compiler generates 2920 Assembly Language Code**
- **Extensive command set for designing electrical filters**
- **Graphics capability enhances analysis of filter response or piecewise linear function approximations**
- **Powerful MACRO capability for executing frequently used routines**
- **Interactive software support tool for 2920 Signal Processor**
- **Extends Intellec® Microcomputer Development System support of the 2920**
- **Contains MACRO library for several standard filters and signal processing functions**

The 2920 Signal Processing Applications Software/Compiler (SPAS20) is an interactive tool for designing software to execute on the 2920 Signal Processor.

The SPAS20 package can be visualized as being comprised of four inter-related sections: A compiler section, a filter design section, a curve fitting section, and a MACRO section.

Among the abilities of SPAS20 are: ability to generate 2920 assembly language code directly from specifications of signal processing building blocks such as filters and waveform generators; ability to generate 2920 assembly language code for several classes of algebraic equations such as $Y = C * X$, $Y = C * Y$, and $Y = C * X + Y$ where X, Y are variables and C is a constant; ability to generate 2920 assembly language code for one variable function $Y(X) = F(X)$; ability to examine time and frequency responses of filter sections specified by continuous or sampled poles and zeroes; ability to examine piecewise linear approximation of specific function; ability for users to implement more complex commands by grouping sets of commonly used commands into a MACRO.

The SPAS20 package runs under ISIS-II on any Intellec® Microcomputer Development System with 64K RAM. The output of SPAS20 can be assembled with the 2920 assembler, tested with the 2920 Simulator, and programmed into the 2920 chip with the Universal PROM Programmer for prototyping.

AFN-01386A

The 2920 Signal Processing Applications Software/Compiler gives the analog designer a "high level language" for his 2920 applications—it decreases the need to code 2920 assembly language. Furthermore, the compiler is interactive. This feature enables the designer to define a filter, or transfer function, graph their response, and change their parameters many times, without having to program and test in an actual 2920 implementation.

Once a filter is realized by moving poles and zeros in the continuous and sampled planes, the filter may be coded and written onto an ISIS file. Similarly, after a function Y = F(X) has been defined, the code for a piecewise linear approximation can be stored onto an ISIS file. Several other file commands are available to store and retrieve command sequences for SPAS20 sessions.

SPAS20 Command Language

DEFINE	This command defines a pole or zero by associating it with a number (i.e., POLE 3), and with real and imaginary coordinates in the continuous or sampled plane. This command also defines a symbol by associating a name with a numeric value, or a MACRO by providing a pointer to a specified command sequence.
GRAPH/ OGRAPH	This command graphically displays the values of object(s) specified. For example, GRAPH GAIN and GRAPH PHASE are used to display filter response. The OGRAPH command will "overgraph" the new response over the old response, after any changes have been made. (You may also graph Group Delay, Step, and Impulse.)
MOVE	Allows the definition of a pole or zero to be changed—its coordinates, its plane, or both.
REMOVE	Deletes the definition of a pole, zero, symbol, or macro.
HELP	Types an explanatory message on the console, pertaining to a command or its attributes.
FIT	This command performs curve fitting, i.e. it approximates an arbitrary user supplied function with a piecewise linear function.
	tion of a set of vertices (i.e. X – Y coordinate pairs) which determine a piecewise linear approximation of some defined function, filter response characteristics, etc.
HOLD	Command to correct attenuation due to sample-and-hold distortion: if ON, it corrects absolute gain by sin(x)/x and phase by adding x, where x=TS*FREQ*π. It corrects group delay by subtracting π*TS.
EVALUATE	Gives the decimal numeric value of any expression.
CODE	Creates 2920 assembly language code for given poles, and zeros, equations, and user defined functions.

The SPAS20 compiler also recognizes the following commands for file handling:

PUT/ APPEND	Writes out objects (commands) to a specified file, either creating a new one or appending an existing one. This enables the user to store all or part of a SPAS20 session on a diskette to be brought back later with the INCLUDE command.
DISPLAY	Copies the contents of a file to the console.
INCLUDE	Executes a sequence of instructions from a diskette file as if they were typed in from the console.
LIST	Creates a file containing all console interactions.

In addition to naming macros for specific command sequences, compound and conditional commands may be formed using all of the above statements. These compound commands are:

IF	Establishes conditional flow of control within a block of commands.
REPEAT	Used for repetition of a block of commands; executes indefinitely or until a condition is met (using WHILE, UNTIL, and END statements).
COUNT	Establishes the number of times a command sequence is to be executed, in a looping fashion.

SPAS20 MACRO Facility

A macro is a sequence of commands that is stored on a temporary diskette file. The command sequence is executed when the macro name is entered as a command. This saves repetitive entry of the sequence, and permits alogorithms to be saved on diskette for future use. This SPAS20 facility allows you to do the following:

- Display the text of any macro.
- Define a macro, specifying its name and any parameters that are to be used by the block. This definition is followed by the contents of the macro (commands) and the EM statement to end its definition.
- Invoke a macro by entering its name and appropriate values for any parameters.
- List the names of all defined macros.
- Remove any or all macros.

Intel also supplies several MACRO library files containing the following commonly needed MACROs:

- Filter design MACROS
 - — Butterworth filter
 - — Chebyshev filter
 - — Bilinear transform
 - — Evaluate gain or phase of digital filter in parallel form
 - — Time response simulation
- Function design MACROs
 - — Code and error optimization
 - — Calculate instertitial error
- MACROs for generation of 2920 code
 - — Code for all-POLE filter
 - — Input and A/D conversion
 - — Multiplication
 - — Division
 - — Logarithm functions
 - — Square-root functions
 - — Sinewave oscillator

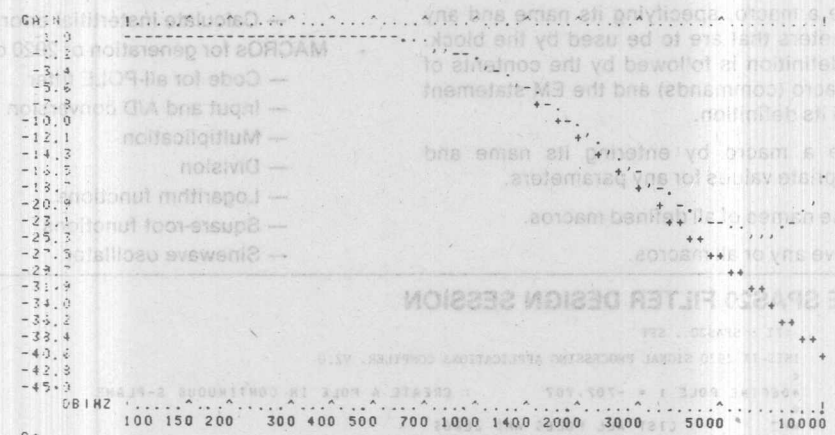
SAMPLE SPAS20 FILTER DESIGN SESSION

```
-:FI : SPAS20 . SFT
ISIS-II 2920 SIGNAL PROCESSING APPLICATIONS COMPILER. V2.0
*
*DEFINE POLE 1 = -707,707        ; CREATE A POLE IN CONTINUOUS S-PLANE
*
*PZ          ; LIST ALL POLES AND ZEROS
POLE 1 = -707.00000,707.00000,CONTINUOUS
*
*FSCALE = 100,10000        ; ESTABLISHES FREQUENCY RANGE OF INTEREST
*
*YSCALE = -45,1        ; ESTABLISHES MAGNITUDE RESPONSE RANGE OF INTEREST
*
*GRAPH GAIN        ; PLOT MAGNITUDE RESPONSE OF POLE PAIR

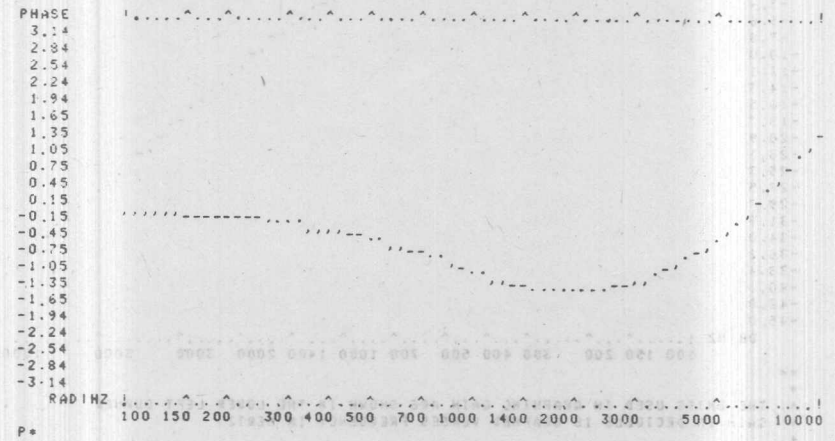
GAIN      !.....^...^...^...^...^...^...^...^...^...^.....^.....^.....!
   1.0    ---------------------------....
  -1.2                                  ''--.
  -3.4                                       '-.
  -5.6                                          '-.
  -7.8                                             '-.
 -10.0                                                '-.
 -12.1                                                   '-.
 -14.3                                                      '-.
 -16.5                                                         '-.
 -18.7                                                            '-.
 -20.9                                                               '-.
 -23.1                                                                  '-.
 -25.3                                                                     '-.
 -27.5                                                                        '-.
 -29.7                                                                           '-.
 -31.9                                                                              '-.
 -34.0                                                                                 '-.
 -36.2                                                                                    '-.
 -38.4                                                                                       '-.
 -40.6                                                                                          '-.
 -42.8                                                                                             '-.
 -45.0
     DB|HZ !.....^...^.....^...^...^....^.....^... ^ ...^.....^.....^.....!
           100 150 200   300 400 500  700 1000 1400 2000  3000    5000     10000
**
*
*; THE UNITS USED IN GRAPHING GAIN ARE SHOWN IN THE LOWER LEFT CORNER.
*; GAIN IN DECIBELS IS GRAPHED VERSES FREQUENCY IN HERTZ
*
*; PREPARE TO MOVE TO THE DIGITAL DOMAIN.
*; SAMPLE RATE MUST BE SPECIFIED.
*
*TS = 1/13020        ; RATE FOR 192 INSTRUCTION PROGRAM AND 10MHZ CLOCK
TS = 7.6805004/10**5
*
```

SAMPLE SPAS20 FILTER DESIGN SESSION (Cont'd.)

```
*MOVE POLE TO Z          ; CONVERT FILTER TO DIGITAL VIA MATCHED-Z TRANSFORMATION
1 POLES/ZEROES MOVED
*
*P          ; LIST TRANSFORMED POLE
POLE 1 = 0.71092836,0.34118369,Z
*
*; COMPARE RESPONSES OF THE ANALOG AND DIGITAL FILTERS BY GRAPHING THE
*; NEW RESPONSE OVER THE OLD
*
*GGRAPH GAIN
```




```
G*
*
*; PLUS SIGNS INDICATE OLD CURVE
*; NOTE THAT THE DIGITAL FILTER RESPONSE BEGINS TO INCREASE AGAIN
*; AT HALF THE SAMPLE RATE ( 6510 HZ )
*
*; THE PHASE CHARACTERISTICS OF THIS FILTER CAN BE EXAMINED
*
*YSCALE = -PI,PI          ; ESTABLISHES RANGE OF INTEREST
*
*GRAPH PHASE
```




```
P*
*
*PUT :F1:POLE PZ          ; SAVE THE POLE LOCATION IN A DISK FILE BACKUP
*
*CODE POLE 1 INST(11      ; GENERATE 2920 ASSEMBLY CODE FOR THIS FILTER
B:=1 33989990  B2=-0.50541914
```

SAMPLE SPAS20 FILTER DESIGN SESSION (Cont'd.)

```
      OPTIMIZED 2920 CODE IS NOW GENERATED  TO SAVE SPACE, SOME
    OF THE SCREEN OUTPUT HAS BEEN DELETED  NORMALLY ALL ATTEMPTS
    BY THE COMPILER TO GENERATE CODE ARE ECHOED ON THE SCREEN  )

INST=10
 POLE 1 = 0.71089458,0.34116779,Z
  BEST: PERROR = 3.3795874/10**5,1.58846567/10**5

; NOTE: MAKE SURE SIGNAL.IS <0.74635571
LDA OUT2_P1,OUT1_P1,R00
    ; OUT2_P1=1.00000000*OUT1_P1
LDA OUT1_P1,OUT0_P1,R00
    ; OUT1_P1=1.00000000*OUT0_P1
SUB OUT0_P1,OUT1_P1,R05
    ; OUT0_P1=1.00000000*OUT0_P1-0.031250000*OUT1_P1
ADD OUT0_P1,OUT0_P1,R03
    ; OUT0_P1=1.12500000*OUT0_P1-0.035156250*OUT1_P1
ADD OUT0_P1,OUT1_P1,R02
    ; OUT0_P1=1.12500000*OUT0_P1+0.21484375*OUT1_P1
SUB OUT0_P1,OUT2_P1,R01
    ; OUT0_P1=1.12500000*OUT0_P1+0.21484375*OUT1_P1-0.50000000*OUT2_P1
SUB OUT0_P1,OUT2_P1,R08
    ; OUT0_P1=1.12500000*OUT0_P1+0.21484375*OUT1_P1-0.50390625*OUT2_P1
ADD OUT0_P1,OUT2_P1,R11
    ; OUT0_P1=1.12500000*OUT0_P1+0.21484375*OUT1_P1-0.50341796*OUT2_P1
SUB OUT0_P1,OUT2_P1,R09
    ; OUT0_P1=1.12500000*OUT0_P1+0.21484375*OUT1_P1-0.50537109*OUT2_P1
ADD OUT0_P1,IN0_P1,R00
    ; OUT0_P1=1.12500000*OUT0_P1+0.21484375*OUT1_P1-0.50537109*OUT2_P1+1.00000000*IN0_P1
*
*; THE CODE COMMAND SPECIFIED THAT THE POLE PAIR BE CODED IN LESS THAN 11
*; INSTRUCTIONS, SO 10 INSTRUCTIONS WERE GENERATED, WITH COMMENTS.
*; THE FINAL ERROR IN RADIUS AND ANGLE FOR THE POLE PAIR WAS OF THE
*; ORDER OF 1/10**5 AS INDICATED ABOVE IN PERROR.
*; THIS OPTIMIZED 2920 ASSEMBLY CODE CAN NOW BE APPENDED TO A FILE
*; WHICH MAY CONTAIN OTHER CODED FUNCTIONAL BLOCKS OF A 2920 PROGRAM
*
*EXIT
```

SAMPLE SPAS20 CURVE FITTING SESSION

```
-;        DEMONSTRATION OF THE SPAS20 CURVE-FITTING PACKAGE
-
-
-SPAS20.SFT

ISIS-II 2920 SIGNAL PROCESSING APPLICATIONS SOFTWARE/COMPILER, V2.0
*LIST XCUBED.829
*
*
*;  THE CURVE FITTING COMMANDS IN SPAS20 WILL GENERATE 2920 CODE TO CALCULATE
*;  SOME FUNCTION SUCH AS  X**3.   X**3 COULD BE COMPUTED ON THE 2920 CHIP
*;  WITH TWO MULTIPLIES USING ABOUT 18 INSTRUCTIONS AND THE DAR.  HOWEVER IT
*;  WOULD TIE UP THE DAR TOO LONG.  THE CODE GENERATED BY THE CURVE FITTING
*;  COMMANDS DOES NOT USE THE DAR.
*
*CODE FIT XSCUBED(X) = X**3 ERROR<.05   ;ERROR BOUND OF .05
*
*CODE     ; HERE IS THE CODE GENERATED.
LDA TEMP,X,R00
    ; TEMP=1.00000000*X
LDA XCUBED,X,R01
    ; XCUBED=0.50000000*X
ADD XCUBED,X,R06
    ; XCUBED=0.51562500*X
ADD TEMP,X,R01
    ; TEMP=0.50000000*X+1.00000000*TEMP
ADD XCUBED,TEMP,R05
    ; XCUBED=1.00000000*XCUBED+0.031250000*TEMP
SUB XCUBED,TEMP,R02
    ; XCUBED=1.00000000*XCUBED-0.21875000*TEMP
ADD TEMP,X,R00
    ; TEMP=1.00000000*X+1.00000000*TEMP
ADD XCUBED,TEMP,R08
    ; XCUBED=1.00000000*XCUBED+0.003906250*TEMP
SUB XCUBED,TEMP,R04
    ; XCUBED=1.00000000*XCUBED-0.058593750*TEMP
LDA XCUBED,XCUBED,L02
    ; XCUBED=4.0000000*XCUBED-0.23437500*TEMP
  *
  *INST     ; THE FUNCTION WAS CODED IN THIS MANY INSTRUCTIONS;
  INST = 10.0000000
  *
```

```
*
*DATA 0 THRU 1   ;EXAMINE THE PIECEWISE LINEAR FUNCTIONS VERTICES.
DATA 0.00000000 THRU 1.00000000 = 0.00000000 AT 0.00000000,&
0.065625012 AT 0.40000000,&
0.26562500 AT 0.66666669,&
0.95312500 AT 1.00000000
*
*GRAPH DATA(X)   ;THE DATA ARRAY APPROXIMATES THE FUNCTION AND CAN BE GRAPHED.
FUNCTION  !.....^.....^.....^.....^.....^.....^.....^.....^.....^.....!
0.95                                                                  _
0.91                                                                _'
0.86                                                              .'
0.82                                                            ,'
0.77                                                          .'
0.73                                                        .'
0.68                                                      _'
0.64                                                    .'
0.59                                                  _'
0.54                                                .'
0.50                                              _'
0.45                                            .'
0.41                                          _'
0.36                                        .'
0.32                                      _'
0.27                                    .-
0.23                                  .-'
0.18                                .--'
0.14                              .--'
0.09                          .--'
0.05                    ....-'
0.00      ...------''''''
          !.....^.....^.....^.....^.....^.....^.....^.....^.....^.....!
*         0.00 0.1    0.2    0.3    0.4    0.5    0.6    0.7    0.8    0.9    1.00
*OGRAPH X**3   ; THE DIFFERANCE BETWEEN THE CODED AND THE ACTUAL APPEARS AS "+".
FUNCTION  !.....^.....^.....^.....^.....^.....^.....^.....^.....^.....!
1.00                                                                  +'
0.95                                                                +'
0.90                                                              +.'
0.86                                                             +.
0.81                                                           ++-
0.76                                                         + -
0.71                                                       +.'
0.67                                                     ++.
0.62                                                   + -
0.57                                                 ++.'
0.52                                               +.-
0.48                                             ++-
0.43                                           +.'
0.38                                         +.'
0.33                                       .'.'
0.29                                     .-'
0.24                                  +.-+
0.19                               ++.-'
0.14                            ++.--'
0.10                         +..--'
0.05                   +++++++...--''
0.00      .............------'''
          !.....^.....^.....^.....^.....^.....^.....^.....^.....^.....!
*         0.00 0.1    0.2    0.3    0.4    0.5    0.6    0.7    0.8    0.9    1.00
*GRA (X**3)-DATA(X)   ; THE ERROR WILL BE GRAPHED.
FUNCTION  !.....^.....^.....^.....^.....^.....^.....^.....^.....^.....!
 0.047
 0.043
 0.039
 0.036                                                                .
 0.032
 0.028                                                  -
 0.025                                                   -
 0.021                                                  .
 0.017
 0.014                                                 - -
 0.010                                                              '
 0.006                                                 -     '
 0.003                                                .          .
-0.001    '.                        .                                '
-0.005      -                      -  '                '
-0.008        '.                  '    -                .            '
-0.012          -                '      '.             '               .
-0.016            '.            .'       '---'.       .-
-0.020              '.        -                        '               -
-0.023                '-.  .-'                          '              .
-0.027                   '''                             '.          .
-0.031                                                     '-..-
          !.....^.....^.....^.....^.....^.....^.....^.....^.....^.....!
*         0.00 0.1    0.2    0.3    0.4    0.5    0.6    0.7    0.8    0.9    1.00
*EXIT   ; THAT'S ALL FOLKS
-
```

2920 ASSEMBLER

2920 program development on Intellec® Microcomputer Development Systems

Translates symbolic assembly language instructions into 2920 machine code

Produces Assembly Listing, Object Code File, and Error Diagnostics

Output used for 2920 programming with the Intellec PROM Programmer or the 2920 Simulator for program debug

The 2920 Assembler translates symbolic 2920 Assembly Language instructions into the appropriate machine operation codes. Through this facility, the programmer is able to symbolically program 2920 hardware operations. Compared to machine code, these symbolic references provide faster programming, easier debugging, and greater reliability.

The Assembler produces an object code file (executable machine code), a complete assembly listing, and error diagnostics. The object code output from the Assembler may be loaded directly into the Intel Universal PROM Programmer for programming the 2920 EPROM. The object code may also be loaded to the 2920 Simulator for 2920 system design and debug.

The 2920 Assembler runs under the ISIS-II Operating System on the Intellec Microcomputer Development Systems.

Sample 2920 Assembly Listing

```
ISIS-II 2920 ASSEMBLER X102                                    PAGE   1

ASSEMBLER INVOKED BY: AS2920 SAW ASM DEBUG

SAWTOOTH WAVE GENERATOR

  LINE  LOC OBJECT  SOURCE STATEMENT

     1            $TITLE('SAWTOOTH WAVE GENERATOR')
     2            ;
     3            ;
     4    0 0000EF      INO                 ; SAMPLE INPUT CHANNEL 0
     5    1 0000EF      INO
     6    2 0000EF      INO
     7    3 008AEB      SUB Y,KP1,INO       ; SIMULTANEOUSLY CALCULATE SAWTOOTH
     8    4 008A0A      SUB Y,KP1,R1,INO    ; BY SUBTRACTING 3/16 FROM Y
     9    5 0044EF      LDA DAR,Y,INO       ; ALSO CHECK SIGN BIT OF Y
    10    6 7A8AED      ADD Y,KP7,CNDS      ; IF Y NEGATIVE START NEXT TOOTH
    11    7 6000EF      CVTS                ; CONVERT SAMPLED INPUT TO DIGITAL (SIGN BIT)
    12    8 7082EF      LDA Y,KP0,CNDS      ; SUPPRESS SAWTOOTH IF INPUT WAS < 0
    13    9 4044EF      LDA DAR,Y           ; PREPARE TO OUTPUT SAWTOOTH
    14   10 4000EF      NOP                 ; ANALOG LEVEL MUST SETTLE
    15   11 4000EF      NOP
    16   12 4000EF      NOP
    17   13 8000EF      OUTO                ; OUTPUT SAWTOOTH
    18   14 8000EF      OUTO
    19   15 8000EF      OUTO
    20   16 5000EF      EOP                 ; PROGRAM WILL END IN THREE MORE INSTRUCTIONS
    21   17 8000EF      OUTO
    22   18 8000EF      OUTO
    23   19 8000EF      OUTO
    24
    25                  END

SYMBOL:                         VALUE:

Y                                  0


ASSEMBLY COMPLETE
ERRORS    =     0
WARNINGS  =     0
RAMSIZE   =     1
ROMSIZE   =    20
```

2920 SIMULATOR

Speeds test and debug of 2920 programs

Simulates 2920 internal operation

Operates on Intellec® Microcomputer Development Systems

Allows users to specify 2920 input signals, and display or alter ROM, RAM, and system variables

Output and internal data can be saved on disk for further analysis.

Provides ability to set breakpoints and to collect trace information

Easy-to-learn commands

The 2920 Simulator is a software facility that provides testing and symbolic debugging of 2920 programs in an Intellec Microcomputer Development Systems environment. The 2920 designers have the capability to specify the 2920 input signals, to set breakpoints, to collect and display 2920 input, output, system variables, and ROM and RAM data values during simulation. The 2920 Simulator accepts the hex format object files produced by the 2920 assembler. Output values and internal trace data may be saved on ISIS-II disk files for further analysis.

Functional Description

2920 Input Signal Specification

The four analog signal inputs to the 2920 processor can be specified as algebraic combinations of basic functions of time. The basic functions are SIN, COS, EXP, LOG, SQR, SAW, SQW, ABS.

2920 Simulation

The simulation of 2920 machine instructions is performed in software. All 2920 internal registers, memory, input values, output values, and other system variables can be examined and modified. The internal processing of the 2920 is simulated. Time constants for the sample and hold capacitators are assumed to be zero. Calculation of input signals is performed in single precision floating point. The speed of simulation varies with the complexity of the input signal, breakpoint setting, and trace condition. Exclusive of I/O time requirements, 2920 instructions will be simulated at a rate of approximately several hundred instructions per second.

Breakpoint Capabilities

After each instruction is simulated, the breakpoint is evaluated to determine whether to stop or continue simulation. Conditional breakpoints are also provided for debugging purposes. Simulation can be manually stopped at any time by pressing the ESC key on the Intellec console.

Trace Capabilities

Based on the qualifier's condition, trace data records can be collected during simulation. The trace data records are stored in Intellec resident memory and are optionally written to the console for display or to a disk file for record.

Symbolic Debugging Capabilities

The 2920 Simulator allows the user to refer to program addresses symbolically. The user can load or save the symbols generated from the hex format object files or created during the debugging session. 2920 program memory in ROM can be disassembled, or filled with assembled instructions.

The 2920 Simulator is designed to provide users with powerful, easy-to-use commands. The user interfaces to the Simulator by entering commands to the Intellec console. The commands consist of one command line, terminated by one of the two line terminators — carriage return or line feed.

The 2920 Simulator offers two types of commands:

Simulation and Control Commands

Command	Operation
Simulate	Starts simulation of the input signals and the 2920 program in simulated ROM memory. Initial setting is "FOREVER."
Trace	Controls the trace selection. Initial setting is "TIME."
Qualifier	Sets qualifier condition during trace. Initial setting is "ALWAYS."
Breakpoint	Sets breakpoint condition during simulation. Initial setting is "NEVER."

Interrogation and Utility Commands

Command	Operation
Display	Displays the values of symbols, RAM, ROM, input, output, registers and system variables.
Change	Alters the values of symbols, RAM, ROM, input, register and system variables.
Base	Establishes the mode of display for output data.
Suffix	Establishes the mode of display for input data.
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Define	Enters symbol name and value to user symbol table.
Console	Controls the console on/off display.
List	Defines list device.
Exit	Returns program control to ISIS-II.
Evaluate	Converts expression to equivalent values in binary, decimal, and hex.
Remove	Deletes symbols from symbol table.
Help	Provides a brief summary of the syntax for the command languages.
Graphics On/Off	Switches output mode between list and graphics.
X Size	Enters horizontal display size.

Keyword References

The 2920 Simulator provides users with keyword references to gain access to all of the numeric valued system variables including simulated 2920's memory, register, status flags and input/output. These keyword references can function as the evaluation command, display command, and change command.

- **2920 Processor Keyword References**

IN0	Analog input 0 in volts
IN1	Analog input 1 in volts
IN2	Analog input 2 in volts
IN3	Analog input 3 in volts
OUT0	Analog output 0 in volts (read only)
OUT1	Analog output 1 in volts (read only)
OUT2	Analog output 2 in volts (read only)
OUT3	Analog output 3 in volts (read only)
OUT4	Analog output 4 in volts (read only)
OUT5	Analog output 5 in volts (read only)
OUT6	Analog output 6 in volts (read only)
OUT7	Analog output 7 in volts (read only)
IN	Sampled and held analog input signal in volts
DAR	Digital to analog register (RAM location 40)
PC	Program counter (integer 1 to 192)
CY	Carry (integer 0 or 1)
OVF	Overflow (integer 0 or 1, read only)
OVE	Overflow enable (integer 0 or 1)

- **Software Simulator Keyword References**

TIME	Elapsed simulated time in seconds (read only)
TQUAL	Time when the qualifier last matched in seconds (read only)
COUNT	Number of instructions simulated since last SIMULATE command (integer, read only)
BUFFERSIZE	Number of trace data records (integer, read only)
TINST	Time between successive instructions in seconds (read only)
SIZE	Number of instructions in program disregarding actual EOP placement
TPROG	Time between successive program passes in seconds
VREF	Reference analog level voltage in volts

The above keyword references are designed to aid 2920 program debugging.

ISIS Compatibilities

The 2920 software simulator runs under the ISIS "submit" facility. The 2920 software simulator uses the ISIS-II line editing capabilities to correct errors in an input line on the Intellec console.

Sample 2920 Simulation Session

```
-
-SM2920.SFT

ISIS-II 2920 SIMULATOR, V1.1
*
*;    THIS IS THE SIMULATION OF THE 'SAWTOOTH GENERATOR'
*
*LIST SRG.LOG        ; LISTS THE SIMULATION SESSION TO AN ISIS FILE
*LOAD SRG.HEX        ; LOAD THE OBJECT CODE INTO THE 2920 SIMUALTOR
*ROM 0 TO 5          ; DISPLAY SRG PROGRAN
ROM 000 = LDA .K,KP5,R00,NOP
ROM 001 = ADD .K,KP1,R05,NOP
ROM 002 = LDA .K,.K,R02,NOP
ROM 003 = SUB .OSC,.K,R00,NOP
ROM 004 = LDA DAR,.OSC,R00,NOP
ROM 005 = ADD .OSC,KP4,L01,CNDS
*TPROG=1/10000        ; SET THE SAMPLE RATE
*TRA=PC,RAM .K        ; SET THE ITEMS TO BE TRACED
*BASE=B               ; DISPLAY THE RESULTS IN BINARY
*SIMULATE FROM 0 TILL COUNT=3 ; SIMULATE THREE INSTRUCTIONS
                                TO VERIFY CONSTANT

   PC                                RAM 0
SIMULATION BEGUN
    1.000000000000000000000000      0.101000000000000000000000
    2.0000000E+0                    0.101000010000000000000000
    3.0000000E+0                    0.001010000100000000000000
SIMULATION TERMINATED
*QUALIFIER=PC=0     ; TRACE EVERY PROGRAM PASS
*TRACE=T,DAR,RAM .OSC ; SET THE ITEMS TO BE TRACED
*RAM .OSC=ONE        ; INITIALIZE THE RAM LOCATION
*BREAKPOINT=T>.00132 ; SIMULATE FOR TWO CYCLES
*BASE=D              ; SET THE BASE TO DECIMAL
*SIMULATE FROM 0     ; BEGIN SIMULATION
   T                  DAR                RAM 1
```

```
SIMULATION BEGUN
     0.00010000          0.83984375          0.84277334
     0.00020000          0.68359375          0.68554683
     0.00030000          0.52734375          0.52832026
     0.00040000          0.36718750          0.37109370
     0.00050000          0.21093750          0.21386714
     0.00060000          0.05468750          0.05664056
     0.00070000         -0.10156250          0.89941396
     0.00080000          0.73828125          0.74218745
     0.00090000          0.58203125          0.58496089
     0.00100000          0.42578125          0.42773433
     0.00110000          0.26953125          0.27050776
     0.00120000          0.10937500          0.11328119
     0.00130000         -0.04687500          0.95605459
SIMULATION TERMINATED
*GRAPH ON              ; SWITCHES THE DISPLAY MODE TO GRAPHICS
*TRACE=T,O,DAR,RAM .OSC,-1,-1,1,1   ; SETS ITEMS TO BE TRACED
*RAM .OSC=ONE          ; INITIALIZE THE RAM LOCATION
*SIMULATE FROM 0
   T                 O                    DAR                 RAM 1      -1
      -1                1                    1
SIMULATION BEGUN
->*                                          1                          *
0 *                                          1                    *     *
. *                                          1                *         *
0 *                                          1            *             *
0 *                                          1        *                 *
0 *                                          1 *                        *
1 *                                        2 1                    3     *
0 *                                          1                *         *
0 *                                          1            *             *
0 *                                          1        *                 *
0 *                                          1    *                     *
  *                                          1  *                       *
  *                                        2 1                        3 *
SIMULATION TERMINATED
*EXIT
-
```

SPECIFICATIONS

Operating Equipment

Required Hardware

Intellec® Microcomputer Development System
—Model 800 or 888
—Series II Model 220, 225, 230
64K Bytes of RAM Memory
One or two Floppy Disk Drives
—Single or Double Density
System Console
—CRT or interactive hard copy device

Required Software

ISIS-II Diskette Operating System

Optional Hardware

Line Printer
iSBC-310 High-Speed Mathematics Unit
Universal PROM Programmer

Optional Software

FORTRAN-80 (Product Code MDS-301)

Documentation Package

2920 Assembly User's Guide (9800987)
2920 Simulator User's Guide (9800988)
2920 Signal Processing Application Compiler User's Guide (121529)

Shipping Media

Flexible Diskettes
—Single and Double Density

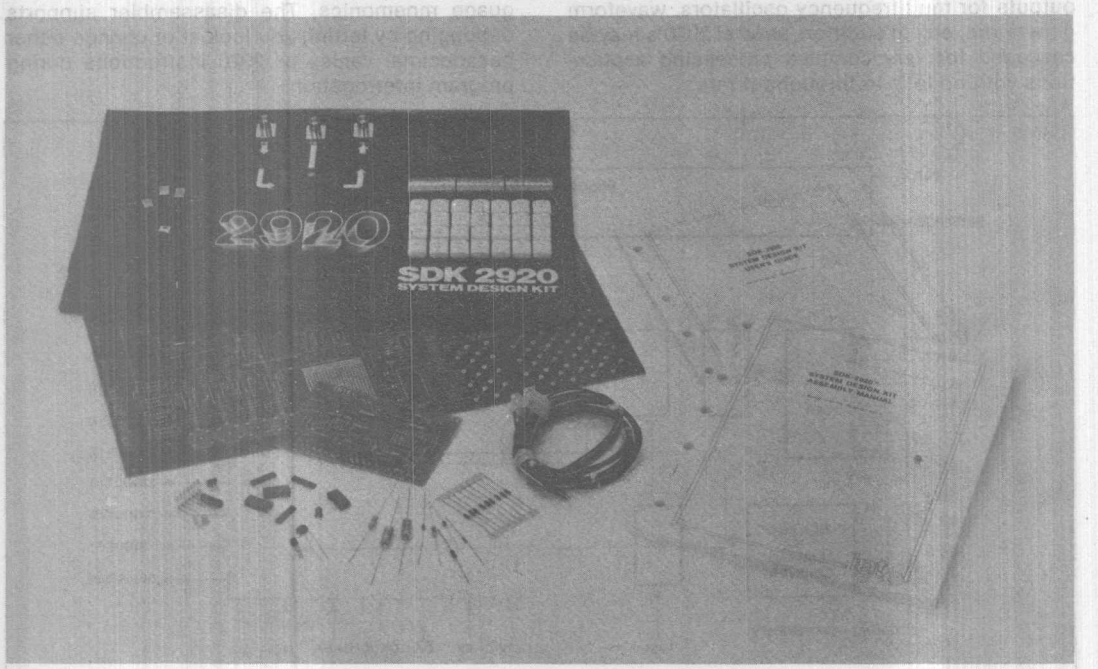
ORDERING INFORMATION

Product Code	Description
MCI-20-SPS	2920 Software Support Package Includes 2920 Signal Processing Application Software/Compiler and 2920 Assembler/Similator Software

SDK-2920
2920 SYSTEM DESIGN KIT

- **Complete 2920 program development:**
 - **— 2920 assembly language keyboard**
 - **— Single-line assembler/disassembler**
 - **— 24-character, alphanumeric display**
 - **— 2920 memory display and modify**
 - **— List program memory to line printer with symbol table**
- **Decimal-to-binary conversion program**
- **File handling capabilities:**
 - **— Up/down load of object file to Intellec or audio cassette**
 - **— Up load source file with symbol table to Intellec**
 - **— 2920 EPROM programming**
- **Real-time execution of a programmed 2920**
- **Breadboarding area**

The SDK-2920 contains all of the components required to assemble a complete single board microcomputer system for programming and evaluation of the 2920 Analog Signal Processor. The 8085/8041A microcomputer-based program development section allows you to immediately enter programs in 2920 assembly mnemonics, translate them to 2920 object code, and program the on-board 2920 EPROM. The kit supports basic filing options such as up/down loading to/from an Intellec, audio cassette, and line printer. The SDK-2920 also provides the user with a 2920 run mode section allowing real-time execution of a programmed 2920. This section comes complete with BNC connectors and Intel's 2912 PCM line filters required for one input and one output network. The kit supports optional input and output circuitry on the run mode section.



FUNCTIONAL DESCRIPTION

The SDK-2920 is a kit which includes all the necessary hardware and software components to assemble, using common laboratory tools and test equipment, a complete single board 2920 programming and evaluation aid. Assembly generally requires 4 to 8 hours, depending on the experience of the user.

The 2920 Signal Processor

The Intel® 2920 Signal Processor is a programmable, single chip analog and digital signal processor specifically designed to replace analog subsystems in real-time processing applications. Its instruction set plus the high precision (25 bits) digital arithmetic logic unit provides the capability to implement very complex subsystems. Typical functions performed by the 2920 include: lowpass and bandpass filters with up to 20 complex pole and/or zero pairs; threshold detectors; limiters; rectifiers; up to 25-bit multiplication and division; approximations to nonlinear functions such as square law and logarithm; logical operations; input and output multiplexing of signals; logical outputs for decision type processing; and analog outputs for multifrequency oscillators, waveform generators, etc. In addition, several 2920's may be cascaded for very complex processing applications with no loss in throughput rate.

Tables 1 and 2 show the 2920 instruction set and op codes.

Table 1. Shift Op Codes

Operation	Mnemonic	Op Code 3	2	1	0	Scale Factor
Shift Right 13 Bits	R13	1	1	0	0	2^{-13}
Shift Right 12 Bits	R12	1	0	1	1	2^{-12}
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
Shift Right 1 Bit	R01	0	0	0	0	2^{-1}
No Shift	R00	1	1	1	1	1
Shift Left 1 Bit	L01	1	1	1	0	2
Shift Left 2 Bits	L02	1	1	0	1	4

System Software

A compact but powerful system monitor is contained in 6K bytes of preprogrammed ROM. The monitor includes system utilities such as command interpretation, user program debugging, and interface controls.

The monitor ROM devices also include a single-line assembler and disassembler. The assembler lets you enter programs in 2920 assembly language mnemonics. The disassembler supports debugging by letting you look at or change either hexadecimal values or 2920 instructions during program interrogation.

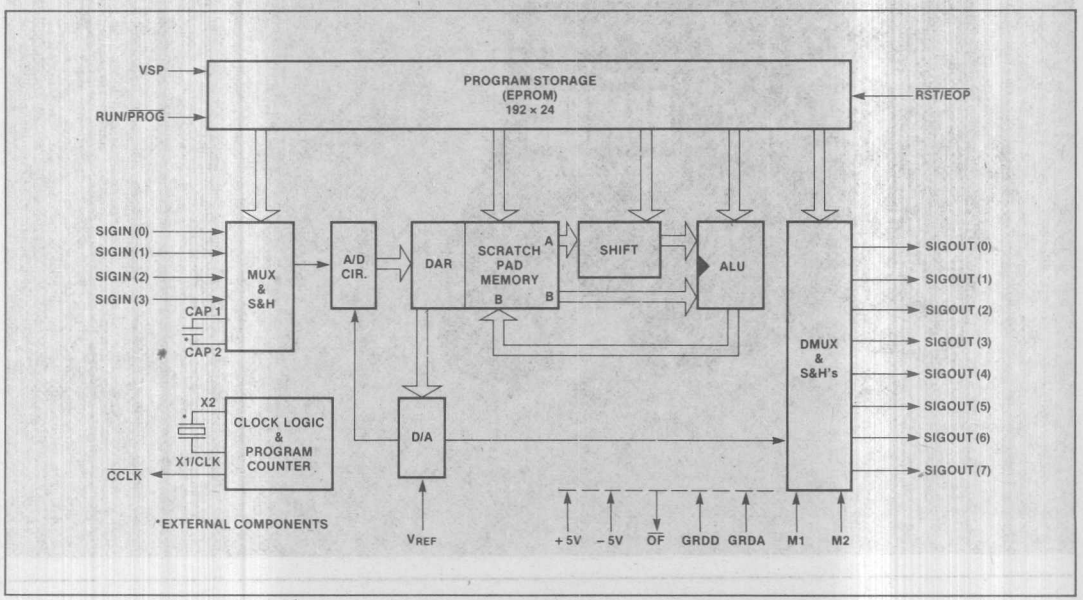
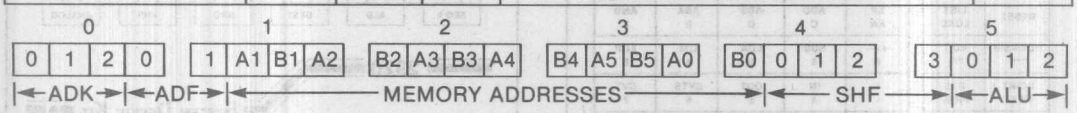


Figure 1. 2920 Function Block Diagram (Run Mode)

Table 2. Instruction Set and Op Codes

Mnemonics / Code Condition	Op Codes[1] ALU	ADF	ADK	Operations	Notes
Digital Instructions	**2,1,0**	**1,0**	**2,1,0**		
ADD	110	↑	↑	$(A \times 2^N) + B \rightarrow B$	
SUB	101			$B - (A \times 2^N) \rightarrow B$	
LDA	111			$(A \times 2^N) + 0 \rightarrow B$	
XOR	000			$(A \times 2^N) \oplus B \rightarrow B$	
AND	001			$(A \times 2^N) \cdot B \rightarrow B$	
ABS	011			$\lvert(A \times 2^N)\rvert \rightarrow B$	
ABA[11]	100	[3]	[3]	$\lvert(A \times 2^N)\rvert + B \rightarrow B$	
LIM	010			$Sign(A) \rightarrow \pm F.S. \rightarrow B$[4]	
ADD CND()[2]	110			$(A \times 2^N) + B \rightarrow B$ IFF DAR(K) = 1 $B \rightarrow B$ IFF DAR(K) = 0	
SUB CND()[2,8]	101			$B - (A \times 2^N) \rightarrow B$ & CY → DAR(K) IFF $CY_P = 1$ $B + (A \times 2^N) \rightarrow B$ & CY → DAR(K) IFF $CY_P = 0$	[5]
LDA CND()[2]	111			$(A \times 2^N) \rightarrow B$ IFF DAR(K) = 1 $B \rightarrow B$ IFF DAR(K) = 0	
ABA[11] CND()[9]	100			$(A \times 2^N) + B \rightarrow B$	
XOR CND()[9]	000			$(A \times 2^N) \oplus B \rightarrow B$	
Analog Instructions					
IN(K)	↑	00	0-3	Signal sample from input channel K	
OUT(K)		10	0-7	D/A to output channel K	
CVTS		00	6	Determine sign bit	
CVT(K)	[7]	01	0-7	Perform A/D on bit K	[6]
EOP		00	5	Program counter to zero	
NOP		00	4	No operation	
CND(K)		11	0-7	Select bit K for conditional instructions	
CNDS	↓	00	7	Select sign bit for conditional instructions	



Note: The input pins for each nibble bit from left to right are D0, D1, D2, D3.

NOTES:

1. Op codes ALU and ADF are in binary notation, ADK is in decimal notation and represents the value "K" when appropriate.
2. CND() can be either CND(K) or CNDS testing amplitude bits or the sign bit of the DAR respectively.
3. Determined by analog instructions below.
4. B is set to full scale (F.S.) amplitude with the same sign as the "A" port operand.
5. The previous carry bit (CY_P) is tested to determine the operation. The present carry bit (CY) is loaded into the Kth bit location of the DAR. "Present carry (CY) is generated independent of overflow. It will represent the carry (CY) of a calculated 28-bit result."
6. EOP will also enable overflow correction if it was disabled during a program pass. The EOP must occur in ROM location 188.
7. Determined by digital instructions above.
8. For SUB CNDS Operation $\overline{CY} \rightarrow DAR(S)$.
9. Does not affect DAR. In this case, CND Is used with XOR/ABA to enable/disable the ALU overflow saturation algorithm. Use of either instruction causes the ALU output to roll over rather than go to full scale with sign bit preserved. An EOP instruction will also enable the ALU overflow saturation algorithm.
10. Clarification of CY_{OUT} sense for certain operations. For LDA, XOR, AND, ABS; $CY_{OUT} \rightarrow 0$.

Memory

The kit contains 1.25K bytes of RAM for 2920 program development. The RAM is used as 2920 program memory for up to a 192-instruction 2920 program. The RAM space is also used for a symbol table up to 40 user defined symbols.

User Interface

The kit includes a function and hex keyboard and a formatted 24-character, 18-segment display for easy 2920 code entry. The interactive keyboard and display enables the system monitor to step the user through a command entry sequence with

the friendliness of a menu-driven operating system.

Optional Interfaces

An RS-232 or 20 mA current loop compatible CRT or printer may be used as a listing or file storage device by connecting it to the board's serial interface connector and supplying + 12 and – 12 volts to the board. In addition, the kit provides an audio cassette interface, allowing the use of an audio cassette as a mass storage device.

Debugging

Program development is made easy by use of interactive error messages that will inform the user of illegal entries at the time of program development. Syntax errors are checked for at time of EPROM programming, giving the user the option to continue the programming or not.

The run-mode section allows the user to execute a programmed 2920 in real time, with his own input stimulus and output circuit or instrumentation. The kit is supplied with the 2920-18 and a 5 MHz crystal (800 ns instructions). However, the kit will support the 2920-16 (600 ns instructions) with a 6.67 MHz crystal or clock.

Assembly and Test

The SDK-2920 assembly manual describes assembly in a step-by-step process that includes checking segments of hardware as they are installed. Building the system requires only a few common tools and standard instruments.

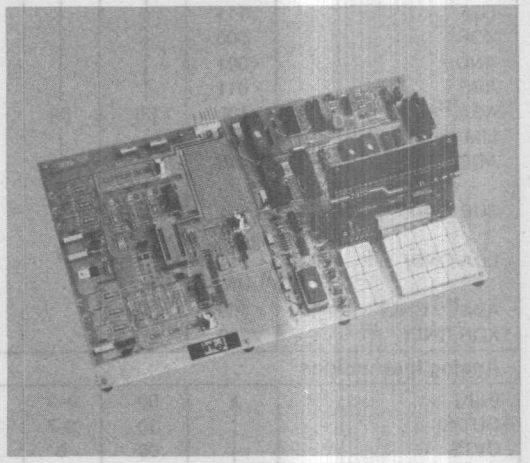


Figure 3. Assembled SDK-2920

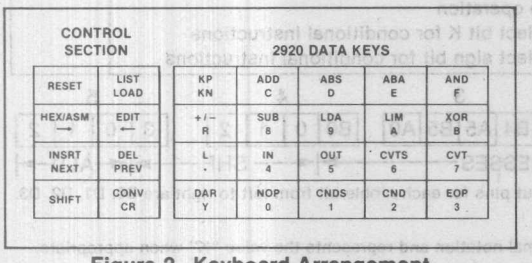


Figure 2. Keyboard Arrangement

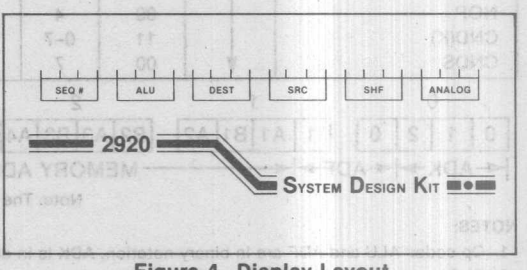


Figure 4. Display Layout

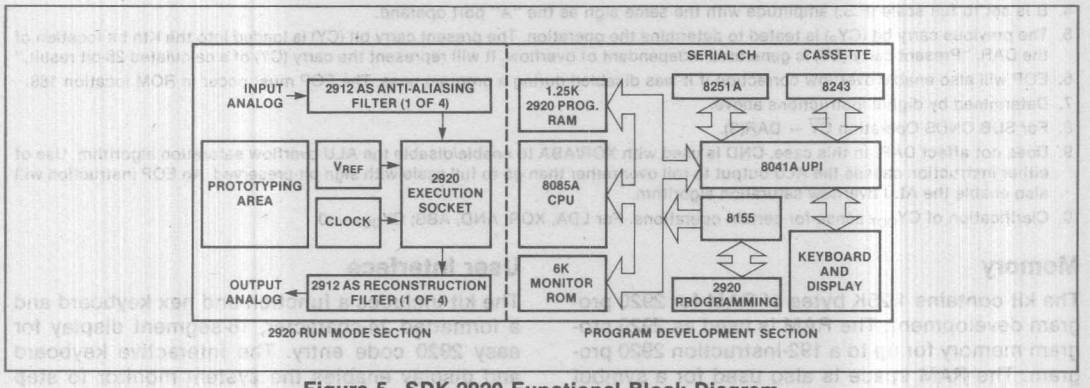


Figure 5. SDK-2920 Functional Block Diagram

Table 3. SDK-2920 Control Commands

RESET	— Sets the monitor to its initialization program and responds to the selection of one of the four modes. The display will prompt the user with EDIT? LOAD? LIST? CONV?.
SHIFT	— Selects the upper case characters or functions.
EDIT	— Selects the edit mode, allowing for 2920 program entry and/or modification. The commands available in the edit mode are shown below in Table 4.
LOAD	— Selects the load mode, providing for up/down loading to/from the RS-232, cassette, or the 20 mA current loop interfaces. It also provides for 2920 EPROM read, program and verify.
LIST	— Selects the list mode, providing for listing the 2920 program source code, symbol table, and 2920 hex code to a line printer via the RS-232 interface.
CONV	— Selects the decimal-to-binary-to-decimal conversion program.

Table 4. Edit Mode Commands

→	Cursor Right	The blinking cursor is moved right one position unless at the end of displayed field.
←	Cursor Left	Blinking cursor is moved left until the sequence number is encountered, then it skips to the left edge of the display.
NEXT	Next Instruction	The next 2920 instruction is displayed unless at end of memory.
PREV	Previous Instruction	The previous 2920 instruction is displayed unless at beginning of memory.
LIST	List Memory	Send disassembled 2920 instructions to serial port.
HEX/ASM	Mode Toggle	Toggle edit mode between symbolic assembly and hexadecimal.
INSRT	Insert Instruction	Expand the program in memory by one location and insert a NOP at current memory display address.
DEL	Delete Instruction	Contract the program in memory by one location and remove the instruction at the current memory display position.

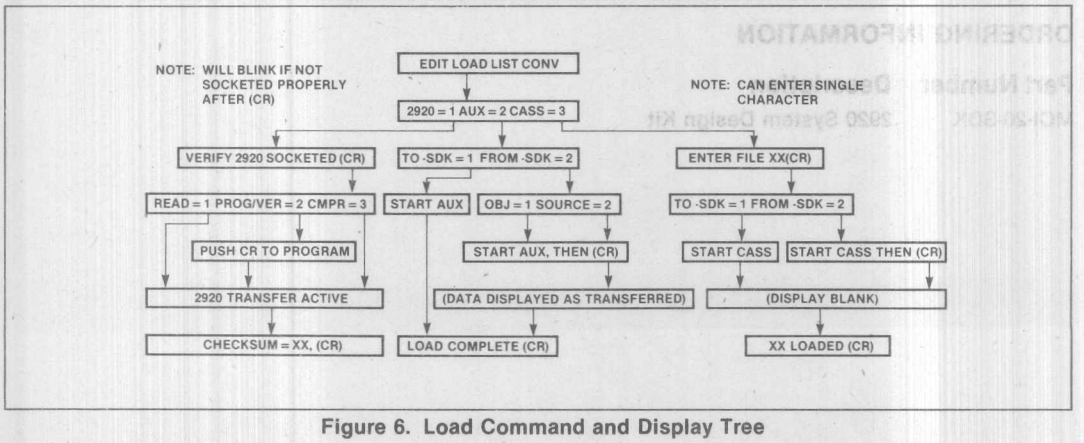


Figure 6. Load Command and Display Tree

SPECIFICATIONS

Control Processor

Intel 8085A microprocessor
6.144 MHz clock rate

Memory

RAM — 1.25K-byte static
ROM — 6K-byte

Interfaces

Keyboard — 28-key with shift, providing 54 functions and characters

Display — 24-character, 18-segment LED

Serial — RS-232 with user-selectable baud rate and 20 mA current loop

Cassette — Hardware and software for audio cassette tape storage interace

Software

System monitor preprogrammed in ROM

2920 assembler and disassembler preprogrammed in ROM

Interface control software preprogrammed in 8041 on-chip ROM

Assembly and Test Equipment Required

- Needle-nose pliers
- Small Phillips screwdriver
- Small flat-blade screwdriver
- Small diagonal wire cutters
- Soldering pencil, <30 watts, 1/16″ diameter tip
- Rosin-core, 60–40 solder, 0.05″ diameter
- Volt-ohm-milliameter, 1 meg ohm input impedance
- Oscilloscope, 1 volt/division vertical sensitivity, 200 μs/division sweep rate, single trace, internal and external triggering

Physical Characteristics

Length — 16 in. (40.64 cm)
Width — 10 in. (25.40 cm)
Height — 4 in. (10.16 cm)
Weight — 3 lb (1.36 kg)

Electrical Characteristics

DC Power Requirements (supplied by user, cables included with the kit)

Program Development Section:

Voltage	Current	Comments
+5V ±5%	1.0A	Required for program development
+12V ±5%	100 mA	Required for 2920 EPROM programming and RS-232 interface
−12V ±5%	100 mA	Required for RS-232 interface

Run Mode Section:

Voltage	Current	Comments
+5V ±5%	300 mA	Required for operation as supplied
	200 mA	Required for each additional 2912/74LS324 pair
−5V ±5%	250 mA	Required for operation as supplied
	200 mA	Required for each additional 2912/74LS324 pair

Environmental Characteristics

Operating Temperature — 0 to 40°C
Relative Humidity — 10% to 90% non-condensing

Reference Manuals

SDK-2920 System Design Kit User's Guide
SDK-2920 System Design Kit Assembly Manual
2920 Analog Signal Processor Design Handbook

ORDERING INFORMATION

Part Number	Description
MCI-20-SDK	2920 System Design Kit

General Information 5

General Information

QUALITY/RELIABILITY

Quality Assurance Operations, Corporate Policy

It is the policy of Intel Corporation to design, manufacture, and deliver products that not only meet our specified standards, but also satisfy our customer standards, and perform reliably in their applications. To this end, Quality Assurance at Intel has the authority to exercise control of quality over every phase of the design and manufacturing process.

Quality Assurance Overview

Since 1969 Intel has been recognized as an innovator and a leader in product quality and reliability—from silicon solutions to system products. This leadership was not achieved by accident. It resulted from a combination of clearly defined objectives, careful planning and thorough execution. At Intel, Quality is a commitment, a philosophy, and a goal: a commitment to satisfy our customer's needs; a philosophy practiced as "do it right the first time"; and a goal of excellence in the world marketplace.

Organization, a Unique Matrix

All product-related Q.A. organizations come under a uniform policy, while still maintaining the flexibility to service the specific needs of a product area. To perform in this manner, a unique matrix organization was developed. All quality and reliability functions report directly through Q.A. operations or site managers to the Director of Quality Assurance. The flexibility is obtained by the Q.A. managers associated with product areas (such as EPROMs, memories, OEM boards, and development systems) also reporting indirectly to (i.e., matrixing to) the operation or division general manager.

Additionally, each product area has both a quality and reliability group under a single Q.A. manager. This involvement on a product-specific level provides both the customer and Intel with the timely response necessary to maintain a problem-free product flow. When problems arise, they are handled quickly on a local level. This results in a "team" approach between quality, reliability, development, and manufacturing—making state-of-the-art technology available in a usable form for our customers.

COMPONENT RELIABILITY

The key to establishing a new product, process or package, or to changing an existing one, is meeting the rigid qualification requirements. Qualification must be run and approved by the appropriate reliability department before any revenue shipment may be made. The reliability goals which have been set during the concept stage must be demonstrated by the qualification. Consider one example, the qualification of a new wafer fab technology for EPROMs. The first 5 wafer lots face the following tests during qualification:

125°C burn-in	168 hours
125°C lifetest	2000 hours
150°C HTRB	1000 hours
*Low-temperature lifetest	1000 hours
250°C storage	1000 hours
Temperature cycle	−65°C to +150°C
Thermal shock	−65°C to +150°C
Test pattern study	
Program/erase cycling	
System verification	

This sequence of tests determines infant mortality, random failure rates, and associated failure mechanisms. This data also becomes the basis of reliability reports made available to our customers.

While successful completion of qualification is the key to product introduction, it would be meaningless if the device were not sampled throughout its product life. On a rotating product basis, 125°C dynamic burn-in and lifetests are performed continuously to monitor all technologies. Fifty thousand devices each month are allocated for the Reliability Monitor Program by the Components Division. In this manner, all generic technology families are continuously scrutinized to assure that reliability goals are met.

In the same manner, Intel Package Reliability performs an extensive package monitor program to assure the mechanical integrity of every package type produced by every assembly facility.

Special Component Quality Programs

The need for an Intel-customer correlation effort has grown with device complexity. In response to this need, a FACR (Failure Analysis Correlation Request) system has been established within each division or operation. Operating through the Field Sales Engineers, the object of the program is to eliminate electrical test discrepancies between Intel and its customers in a timely manner. The system provides direct contact with a product-oriented Quality Engineer to eliminate test program or equipment discrepancies between the customer and Intel without returning all products shipped. The success of the program may be measured by the number of lots that have been shipped to customers and been questioned and accepted after utilizing the FACR system. The obvious by-product of this system is to build customer confidence to the point where Intel's final test and FQA data becomes the customer's incoming inspection data.

Military

The Military Quality Assurance program, operated out of the Phoenix site, attends to customers within the aerospace or military industry, or in some cases, to customers that have special documentation requirements. To perform in this product area, the Military Q.A. acts as an overlay on all sites and operations, defining the Q.A. program requirements in that particular area. The success of this program may be gauged by the acceptance of selected high-technology products by the Federal Government under Mil-M-38510, and the product processing areas certified by an agency of the Federal Government (see "Military Grade Products" for details). This department also performs process audits on a regular basis of applicable Intel manufacturing facilities to assure compliance to rigid military traceability and process requirements.

EXPRESS Program

The EXPRESS burn-in program provides additional testing of components to meet specific customer application requirements. A 168-hour dynamic burn-in at 125°C enables microprocessors, RAMs, EPROMs, and peripheral components to meet high reliability, harsh environment requirements. Customers can also specify testing over two operating ranges—0° to 70°C or −40° to 85°C. The EXPRESS service is available at either temperature range, with or without the extended burn-in. The service applies to products sold in molded plastic packages and hermetic ceramic packages.

SYSTEM QUALITY ASSURANCE

The Systems Quality Assurance Organization is a centralized function with operational entities at each System Site. The Site Quality Assurance Managers have accountability to product General Managers, but report to the Group Quality Assurance Director.

This structure provides unique leverage and significant synergy from a variety of prospectives: most significant is that Product Quality is assured and never compromised.

Operationally the organizations are integrally involved in all phases of product life cycle, and in the control of all internal practices and disciplines.

Organizationally the function at all Sites is composed of 4 entities, each responsible for distinct and measurable tasks, specifically:

1. *Advanced Reliability and Quality Assurance*—responsible for the design reliability of new products, including reliability and environmental qualification, and field reliability performance.

2. *Material Quality Assurance*—responsible for the quality of all procured items, comprising supplier and part qualification, and incoming material testing and control.

3. *Product Quality Assurance*—responsible for the control of all processes during the manufacturing cycle and the quality levels of all outgoing products.

4. *Components Engineering*—responsible for the qualification and selections of electronic parts used in the design of all system products.

Controlling product quality and reliability is a complex task requiring a high degree of integration, organizational involvement and use of specialized disciplines, notably:

Design control through part selection and application, design rules, circuit analysis, derating requirements and assiduous environmental and reliability qualification testing.

Procured material quality through a rigorous supplier selection, qualification and monitoring process. Our computerized control system automatically assures procurement only from selected and approved sources. The right for any supplier to be on the approved list must be earned!

Product quality level monitoring and control through our automated reporting and analysis systems, and improvement through a corrective action system including impositions of extensive product failure free burn-in requirements. But the final measure of outgoing quality is our continuous product sampling program, where a significant percentage of finished products is subjected to a "customer audit". Only products which meet the stipulated quality levels may ship.

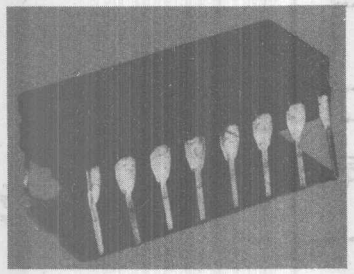
To complete the cycle, a full field reliability reporting system provides timely feedback on our ability to control the product design and manufacturing processes.

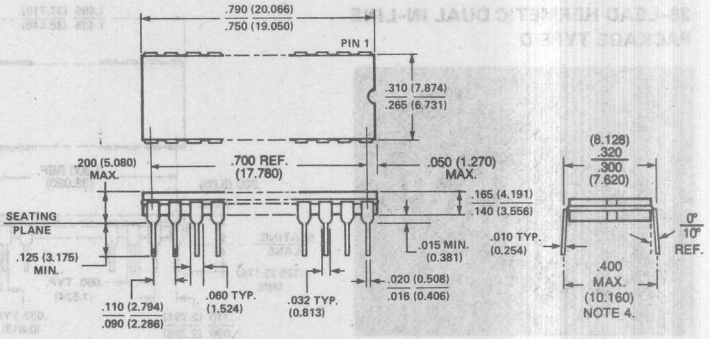
Our approach to quality is based on a very fundamental premise: DO IT RIGHT THE FIRST TIME, while our quality philosophy is structured on two basic precepts: *OUR PRODUCT MUST MEET THE CUSTOMERS NEEDS AND BE IN ABSOLUTE COMPLIANCE TO SPECIFICATIONS.*

To provide you with additional insight on how the Intel Systems Group operates and assures quality of all products and services a video tape presentation has been made available. The name of this production is "INTEL SYSTEMS – SUCCESS BY DESIGN", and can be readily obtained from your Distributor or Intel Salesperson.

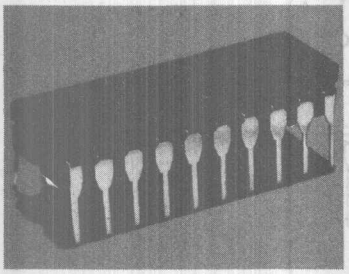
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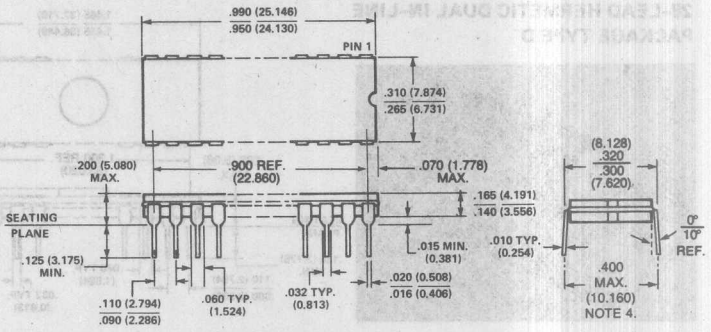
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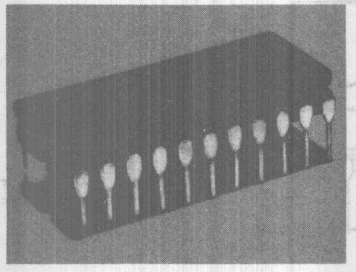


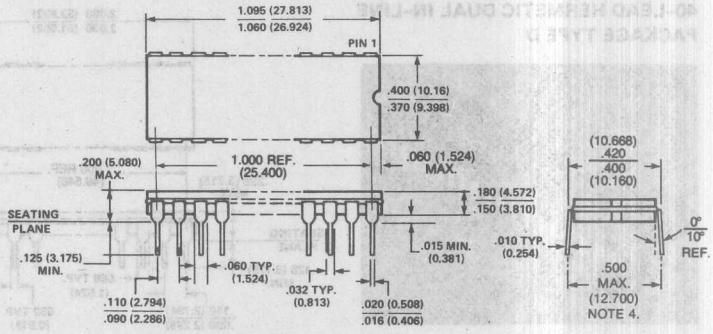
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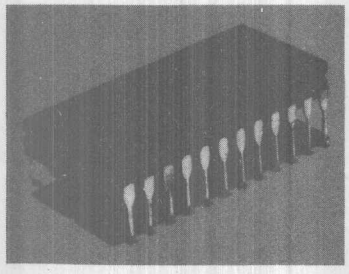


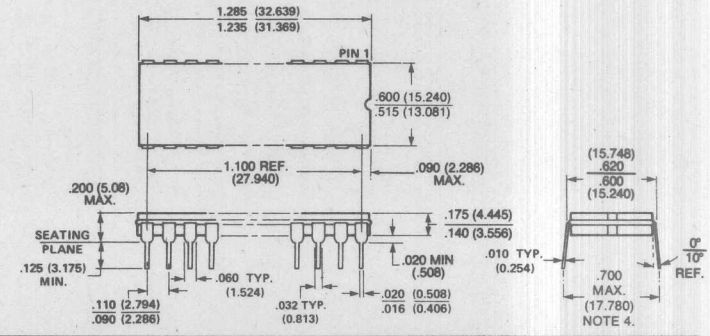
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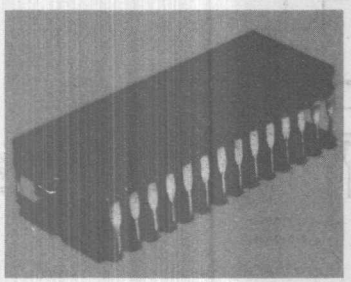


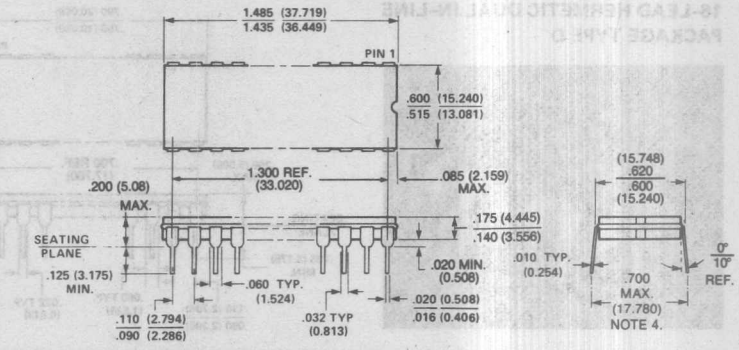
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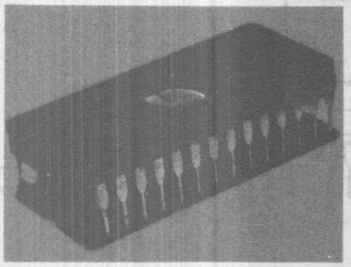


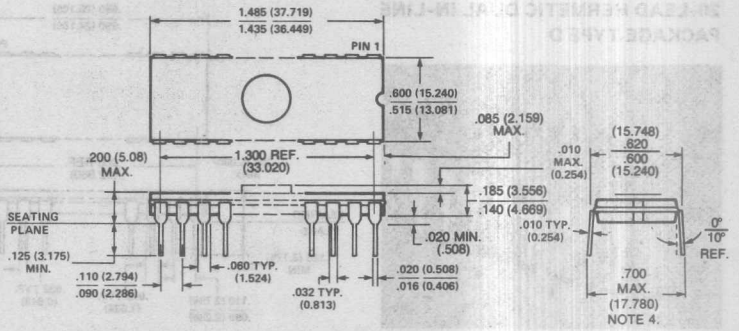
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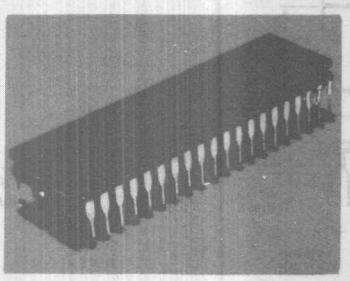


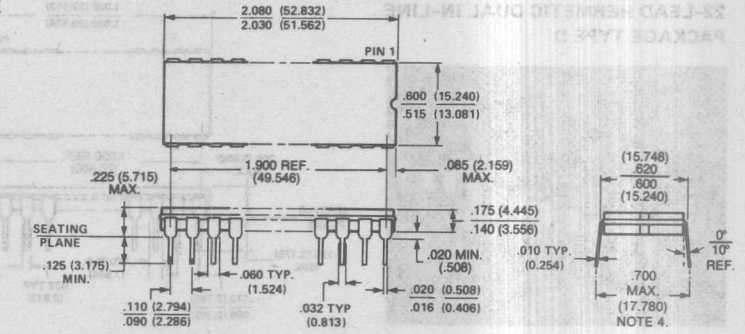
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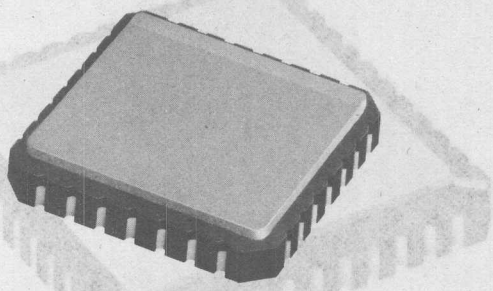


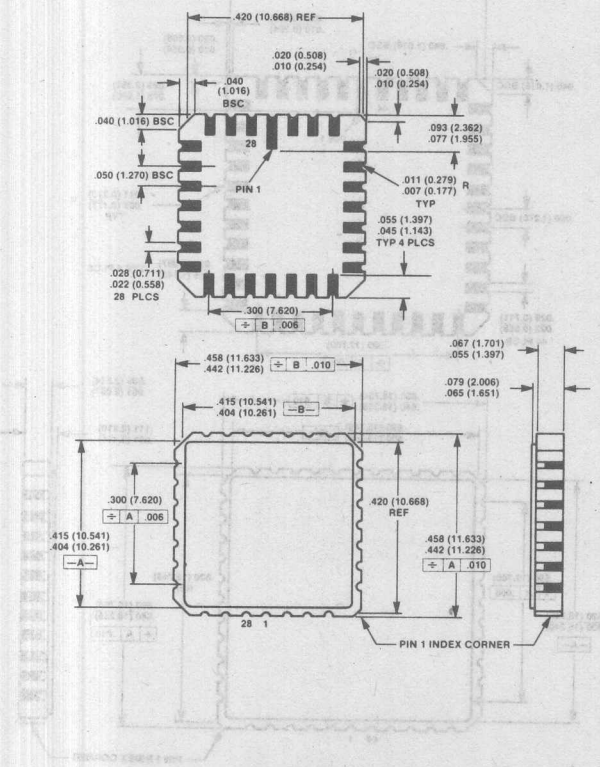


CERAMIC LEADLESS CHIP CARRIER

All dimensions in inches and (millimeters)

28-Leadless Hermetic Chip Carrier
JEDEC Package Type C





CERAMIC LEADLESS CHIP CARRIER

All dimensions in inches and (millimeters)

44-Leadless Hermetic Chip Carrier
JEDEC Package Type C

